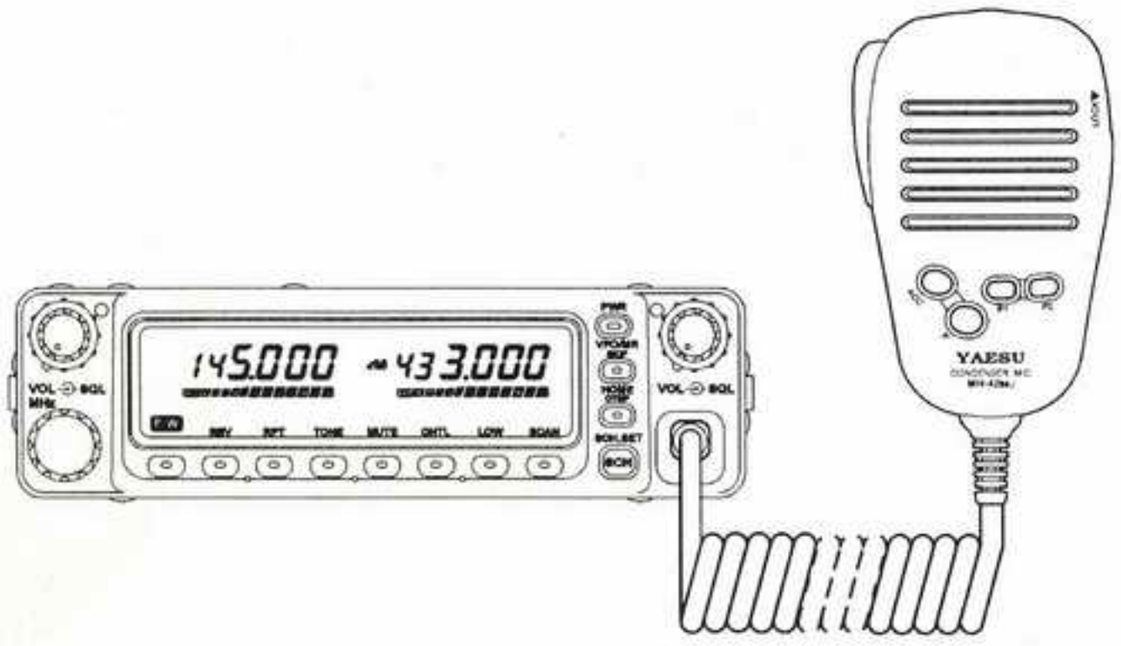
YAESU

FT-8000R

Technical Supplement



YAESU MUSEN CO., LTD.
1-20-2 Shimomaruko, Ota-Ku, Tokyo 146, Japan

YAESU U.S.A.
17210 Edwards Rd., Cerritos, CA 90703, U.S.A.
YAESU INTERNATIONAL DIVISION, (Caribbean, Mexico, Central & So. America)
7270 NW 12th St., Suite 320, Miami, FL 33126, U.S.A.

YAESU EUROPE B.V.
Snipweg 3, 1118DN Schiphol, The Netherlands

YAESU UK LTD.
Unit 2, Maple Grove Business Centre,
Lawrence Rd., Hounslow, Middlesex, TW4 6DR, U.K.

YAESU GERMANY GmbH
Am Kronberger Hang 2, D-65824 Schwalbach, Germany

YAESU HK LTD.
11th Floor Tsim Sha Tsui Centre, 66 Mody Rd.,
Tsim Sha Tsui East, Kowloon, Hong Kong

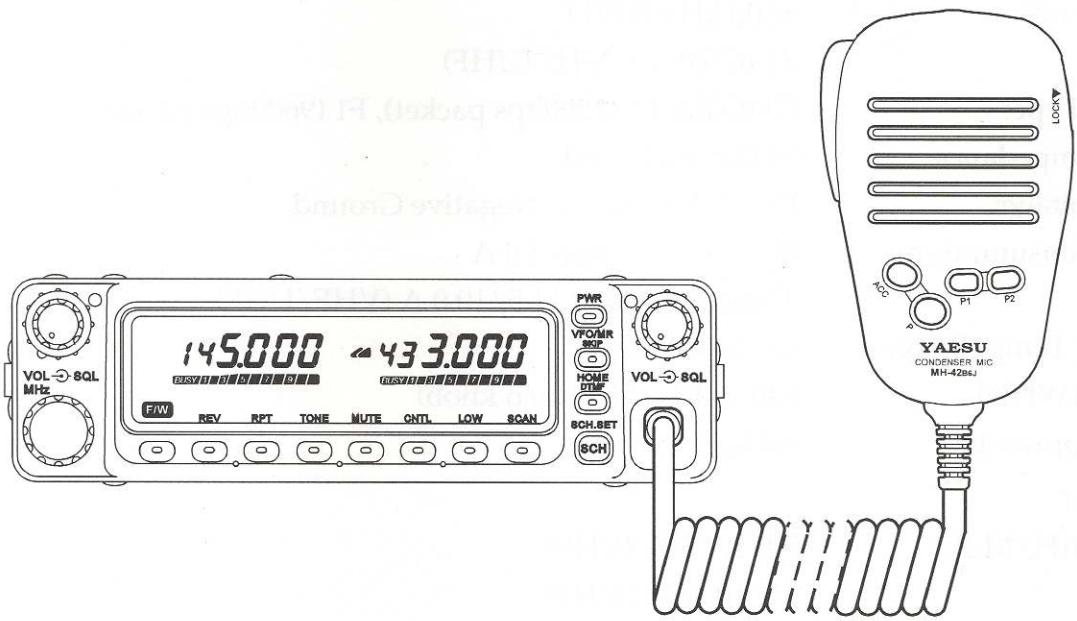
Contents

General Information and Alignment **1**
Introduction 1-1
Specifications 1-2
Chip Component Information 1-3
Exploded View & Miscellaneous Parts 2-1
Alignment 2-3

Servicing **3**
Circuit Description 3-1
Block Diagram 3-7
Interconnection Diagram 3-8

Board Units (Circuit Diagram, Parts Layout, Parts List) **4**
144-VCO Unit 4A-1
430-VCO Unit 4B-1
VR-L Unit 4C-1
VR-R Unit 4D-1
144-Main Unit 4E-1
430-Main Unit 4F-1
CNTL Unit 4G-1
Panel Unit 4H-1

Optional Board Unit (Circuit Diagram, Parts Layout, Parts List) **5**
FTS-22 Tone Squelch Unit 5A-1
MH-36B6J DTMF Microphone 5B-1
MH-42B6J Hand Scanning Microphone 5C-1



The manual provides the technical information necessary for servicing the FT-8000R Dual-Band mobile amateur transceiver.

Servicing this equipment requires expertise in handling surface-mount chip components. Attempts by non-qualified persons to service this equipment may result in permanent damage not covered by the warranty, and may be illegal in some countries.

Two PCB layout diagrams provided for each double-sided board in this transceiver. Each side of the board is referred to by the type of the majority of components installed on that side ("leaded" or "chip-only"). In most cases one side has only chip components, and the other has either a mixture of both chip and leaded components (trimmers, coils, electrolytic capacitors, ICs, etc.), or leaded components only.

While we believe the information in this manual to be correct, Yaesu Musen assumes no liability for damage that may occur as a result of typographical or other errors that may be present. Your cooperation in pointing out any inconsistencies in the technical information would be appreciated.

Specifications

General

Frequency Range:	(RX) 110 ~ 280 MHz, 280 ~ 550 MHz, 750 ~ 1300 MHz*	*: cellular blocked
	(TX) 144 ~ 148 MHz, 430 ~ 450 MHz	
Channel Step:	5*/10/12.5/15*/20/25/50 kHz	*: not available on UHF band
Frequency Stability:	±5 ppm (-5 °C ~ +50 °C)	
Repeater Shift:	±600 kHz (VHF)	
	±1.6/5.0/7.6 MHz (UHF)	
Emission Type:	F3 (G3E), F2 (1200bps packet), F1 (9600bps packet)	
Antenna Impedance:	50 Ω unbalanced	
Supply Voltage:	DC 13.8 V ±15 %, Negative Ground	
Current Consumption:	Receive; less than 1.0 A	
	Transmit (Max); 11.5/10.0 A (VHF/UHF)	
Operating Temp. Range:	-20 to +60 °C	
Case Size (WHD):	140 × 40 × 152 (w/o knob)	
Weight (approx.):	1.0 kg	

Transmitter

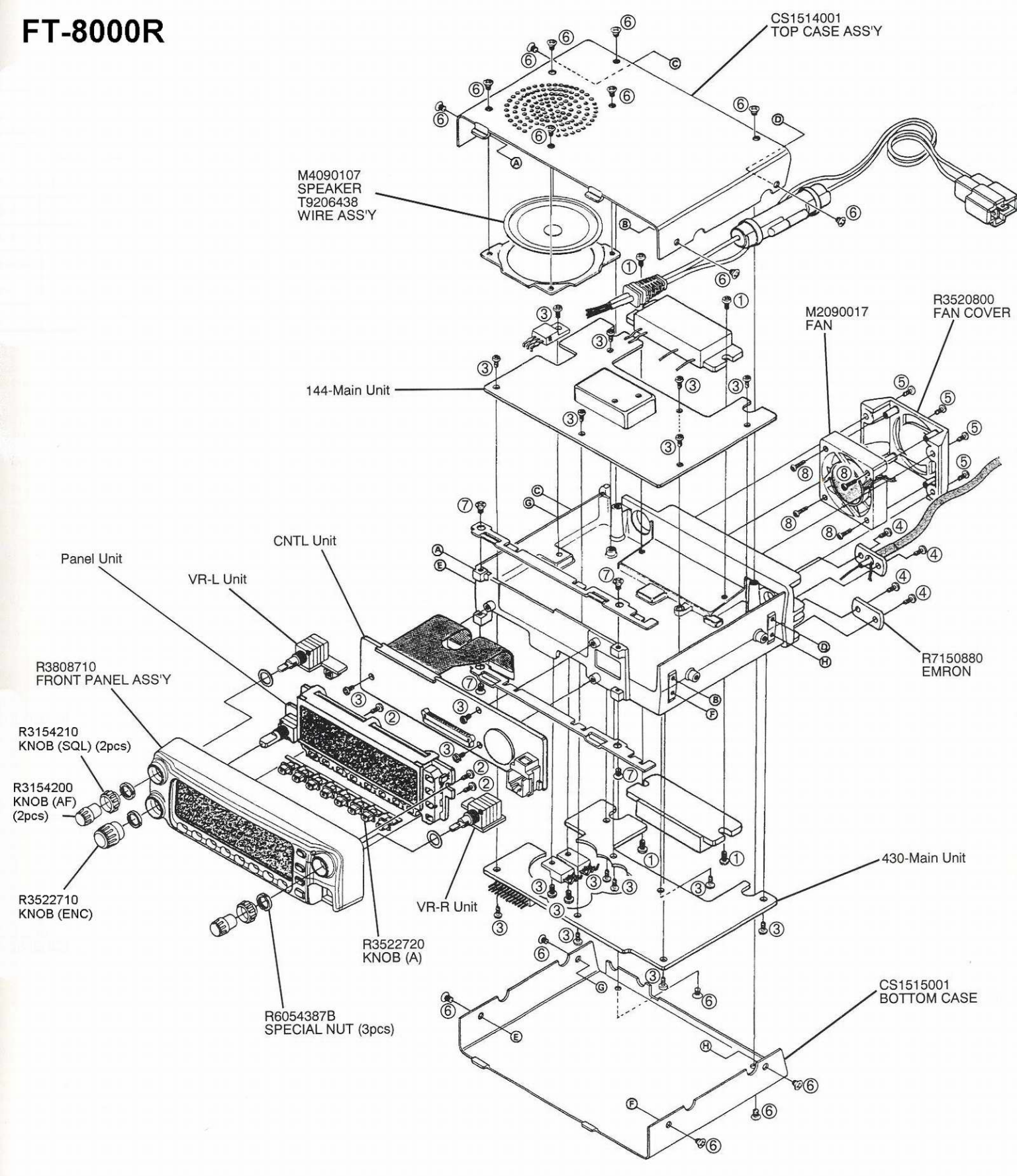
RF Output(H/M/L):	50/10/3 W (VHF)
	35/10/3 W (UHF)
Modulation Type:	Variable reactance
Max Deviation:	±5 kHz
Spurious Emission:	>60 dB below carrier
Distortion (@ 70% MOD.):	less than 3%
Microphone Impedance:	600 ~ 10 kΩ

Receiver

Circuit Type:	Double-conversion superheterodyne
IFs:	45.05 MHz/455 kHz (VHF)
	58.525 MHz/455 kHz (UHF)
12 dB SINAD Sensitivity:	<0.18 μV (MAIN)
	<0.25 μV (SUB)
Selectivity (-6/-60dB):	12/24 kHz
Image Rejection:	better than 70 dB
Squelch Sensitivity:	better than 0.13 μV
AF Output:	2W @ 8 Ω for 5% THD
AF Output Impedance:	4 ~ 16 Ω (8 Ω internal speaker)

Specifications subject to change without notice or obligation.
Specifications guaranteed within amateur bands only.
Frequency range and repeater shift vary according to transceiver version.

FT-8000R


CS1514001
TOP CASE ASS'Y
M4090107
SPEAKER
T9206438
WIRE ASS'Y
144-Main Unit
M2090017
FAN
R3520800
FAN COVER
R7150880
EMRON
CNTL Unit
Panel Unit
VR-L Unit
R3808710
FRONT PANEL ASS'Y
R3154210
KNOB (SQL) (2pcs)
R3154200
KNOB (AF)
(2pcs)
R3522710
KNOB (ENC)
R3522720
KNOB (A)
R60054387B
SPECIAL NUT (3pcs)
VR-R Unit
430-Main Unit
CS1515001
BOTTOM CASE

Alignment Preparation & Precautions

A 50-Ω dummy load and inline wattmeter must be connected to the antenna jack in all procedures that call for transmission, except where specified otherwise. Correct alignment is not possible with an antenna.

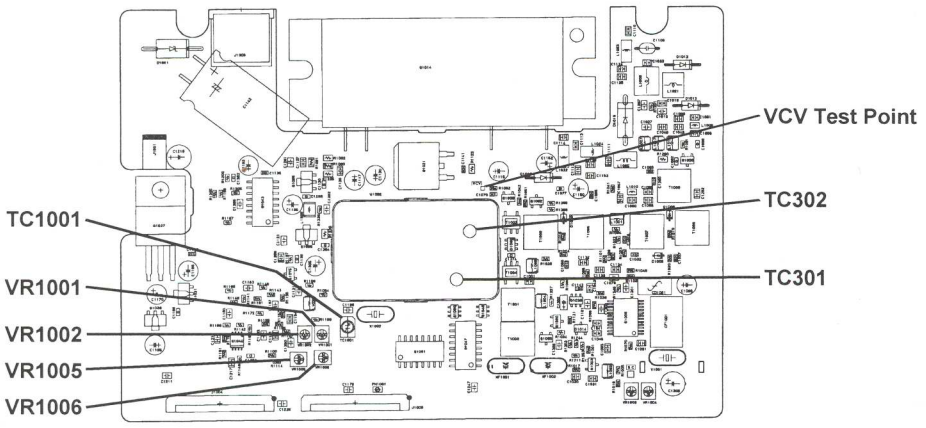
After completing one step, read the following step to determine whether the same test equipment will be required. If not, remove the test equipment (except power supply, dummy load and wattmeter, if connected) before proceeding.

Correct alignment requires that the ambient temperature be the same as that of the transceiver and test equipment, and that this temperature be held constant between 20 and 30 °C (68 ~ 86 °F). If the transceiver is brought into the shop from hot or cold air it should be allowed some time for equalization with the environment before alignment.

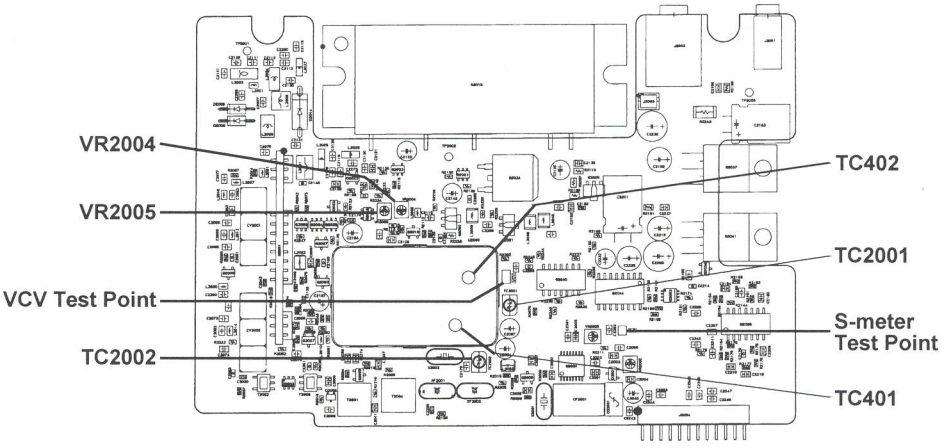
Whenever possible, alignments should be made with oscillator shields and circuit boards firmly affixed in place. Also, the test equipment must be thoroughly warmed up before beginning.

Most alignment procedures call for tuning the transceiver to the high or low band edge, or to band center. The actual frequency differs between different versions, so the technician should make sure of the band limits of each set to be aligned before beginning.

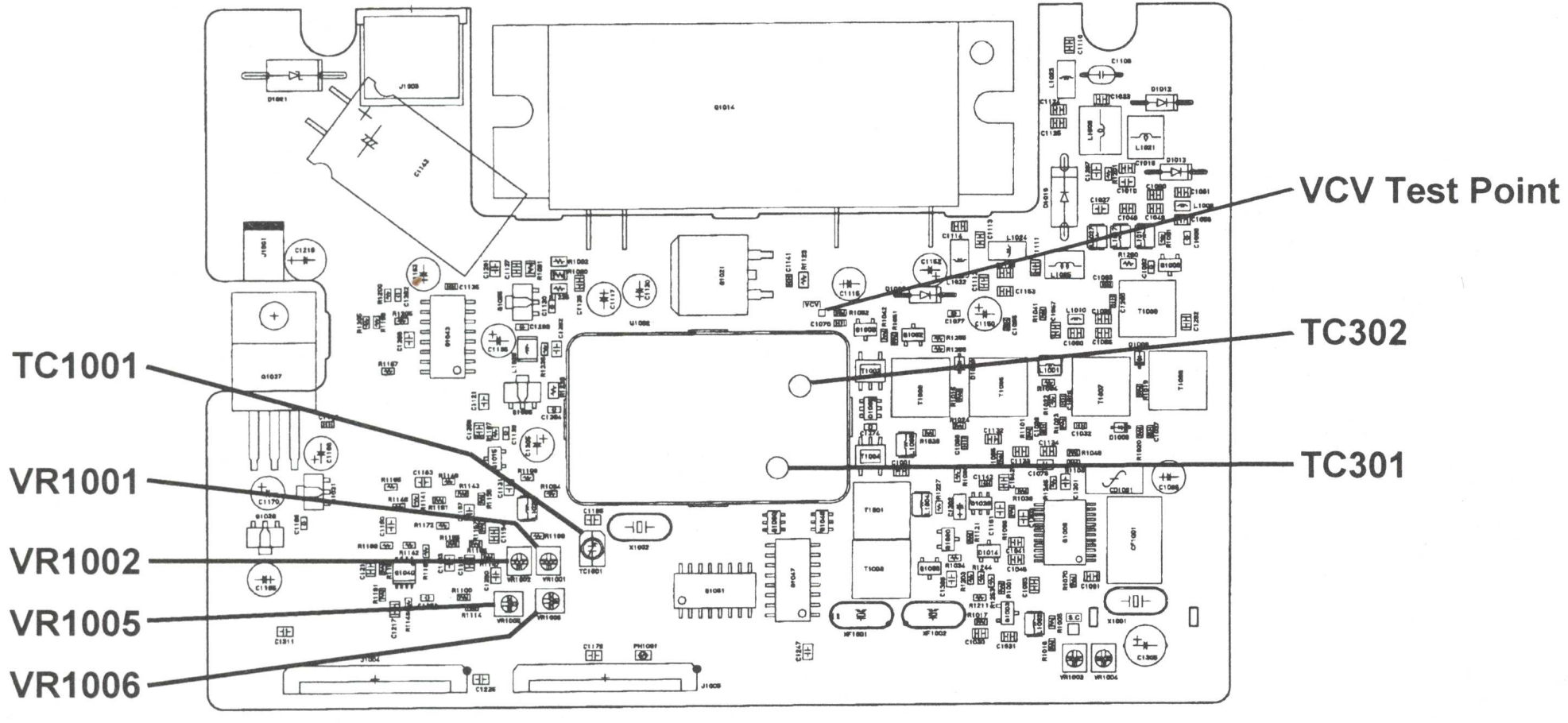
Note: Signal levels in dB referred to in the alignment procedure are based on 0 dBμ = 0.5 dBμV.



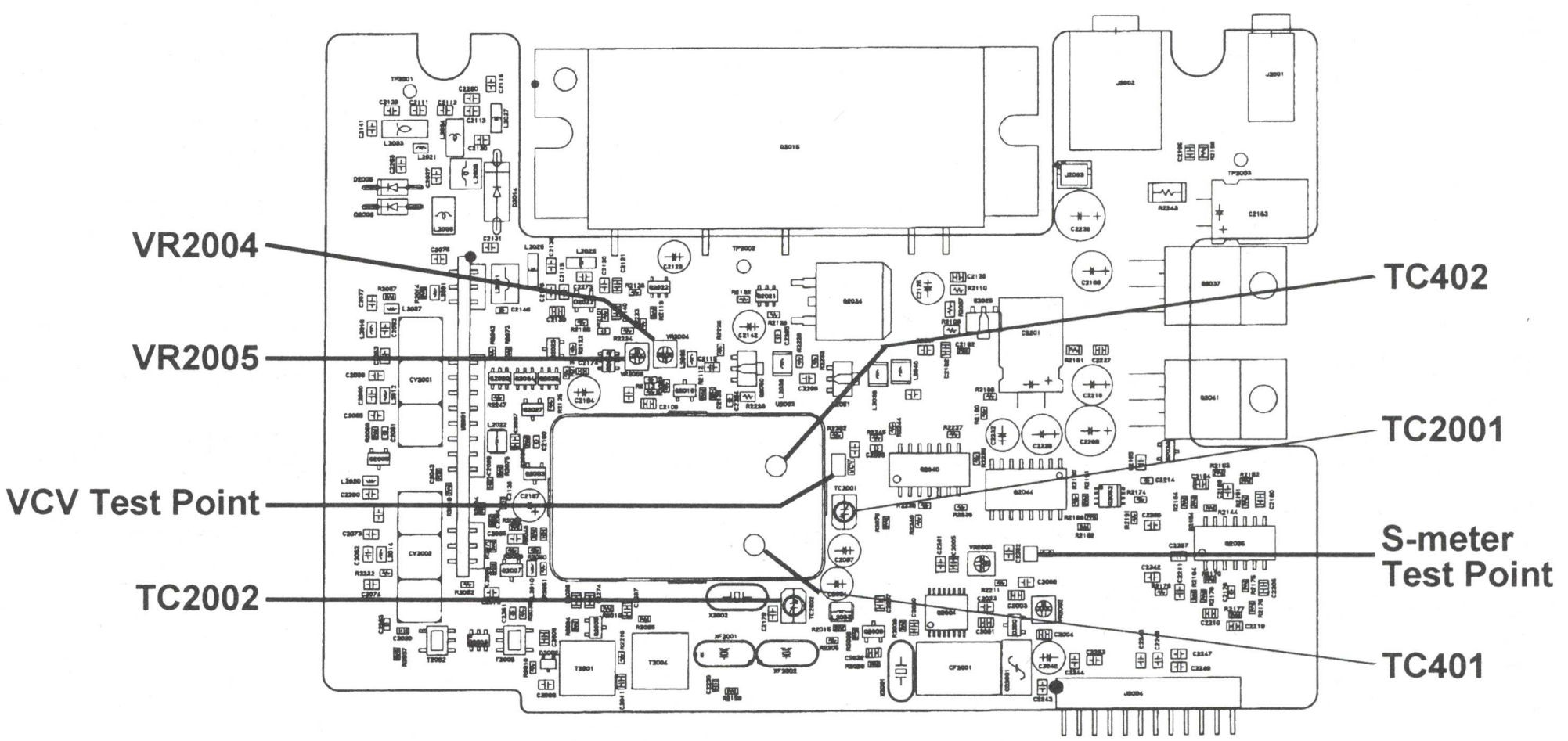
VHF PLL & Transmitter Alignment Points



UHF PLL & Transmitter Alignment Points



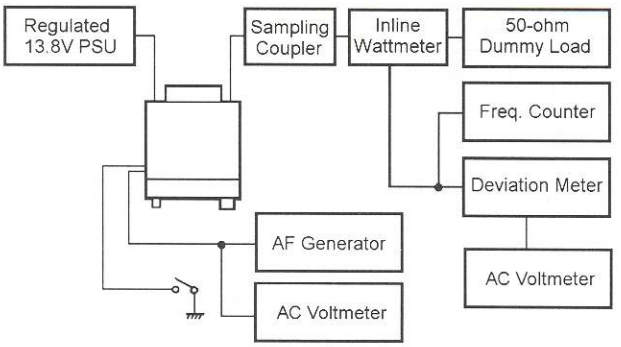
VHF PLL & Transmitter Alignment Points



UHF PLL & Transmitter Alignment Points

PLL & Transmitter

Set up the test equipment as shown for transmitter alignment. Maintain the supply voltage at 13.8V DC for all steps.



Transmitter Alignment Setup

PLL VCV (Varactor Control Voltage)

VHF Band

❑ Connect Voltmeter between **VCV** test point on the 144-Main Unit and chassis ground.

❑ Refer to the chart below, transmit and adjust **TC302** on the 144-VCO Unit for the indicated voltage at that listed frequency. Adjust **TC301** as necessary for the required voltage while receiving.

Rx & Tx VCV Alignment Data							
Main Band				Sub Band			
Frequency		Voltage		Frequency		Voltage	
Rx	TX	Rx	TX	Rx	TX	Rx	TX
146	146	3.5V	2.0V	–	–	–	–
440	440	2.5V	4.0V	145	–	2.5V	–

UHF Band

❑ Connect Voltmeter between **VCV** test point on the 430-Main Unit and chassis ground.

❑ Tune to the required channel, transmit and adjust **TC402** on the 430-VCO Unit for the voltage indicated in the table.

❑ While receiving, adjust **TC401** for the corresponding voltage for that frequency.

❑ Next, set the transceiver SUB band, and adjust **TC2001** on the 430-Main Unit for the voltage indicated in the table.

Transmitters

VHF Power Output

❑ Couple the frequency counter to sample the RF output.

❑ Tune to band center (for the version being aligned), and press the **LOW** button if necessary, to select low power output.

❑ Key the transmitter and adjust **TC1001** on the 144-Main Unit to match the display to the counter frequency (within 100 Hz).

❑ Tune to band center (for the version being aligned), and press the **LOW** button , if necessary, to select high power output.

❑ Key the transmitter and adjust **VR1001** on the 144-Main Unit for 50 watts on the wattmeter.

❑ Press the **LOW** button to select **MID** power, key the transmitter, and confirm 7 to 13 watts on the wattmeter.

❑ Press the **LOW** button to select **LOW** power, key the transmitter and adjust **VR1002** on the 144-Main Unit for 2.5 to 3.5 watts on the wattmeter.

VHF Transmitter Deviation

❑ While tuned to the center of the band, adjust the AF generator attenuator for 50 mV output at 1 kHz to the MIC jack.

❑ Key the transmitter and adjust **VR1006** on the 144-Main Unit for ±4.5 kHz (Vers. USA ±4.0 kHz) deviation on the deviation meter.

❑ Reduce the AF injection until the deviation meter shows ±3.0 kHz deviation, and confirm that the injection level is 5 mV.

UHF Power Output

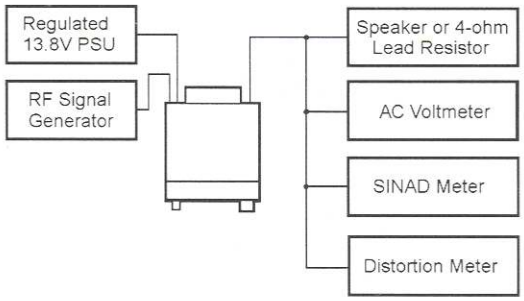
- ❑ Couple the frequency counter to sample the RF output.
- ❑ Tune to band center (for the version being aligned), and press the **LOW** button if necessary, to select low power output.
- ❑ Key the transmitter and adjust **TC2002** on the 430-Main Unit to match the display to the counter frequency (within 100 Hz).
- ❑ Tune to band center (for the version being aligned), and press the **LOW** button , if necessary, to select high power output.
- ❑ Key the transmitter and adjust **VR2004** on the 430-Main Unit for 35 watts on the wattmeter.
- ❑ Press the **LOW** button to select **MID** power, key the transmitter, and confirm 7 to 13 watts on the wattmeter.
- ❑ Press the **LOW** button to select **LOW** power, key the transmitter and adjust **VR2005** on the 430-Main Unit for 2.5 to 3.5 watts on the wattmeter.

UHF Transmitter Deviation

- ❑ While tuned to the center of the band, adjust the AF generator attenuator for 50 mV output at 1 kHz to the MIC jack.
- ❑ Key the transmitter and adjust **VR1005** on the 144-Main Unit for ±4.5 kHz (Vers. USA ±4.0 kHz) deviation on the deviation meter.
- ❑ Reduce the AF injection until the deviation meter shows ±3.0 kHz deviation, and confirm that the injection level is 5 mV.

Receivers

Set up the test equipment as shown here for receiver alignment.



Receiver Alignment Setup

VHF Interstage Transformers

- ❑ Connect Voltmeter between S-mater test point on the 144-Main Unit and chassis ground.
- ❑ Tune the transceiver and RF signal generator to the center of the VHF band. Modulate the RF signal generator with ±3.5 kHz deviation of a 1 kHz tone.
- ❑ Adjust **T1003** and **T1005 ~ T1008** on the 144-Main Unit for maximum voltage on the voltmeter.
- ❑ Confirm -8 dBμ or better 12 dB SINAD at the high and low band edges.

UHF Interstage Transformers

- ❑ Connect voltmeter between S-mater test point on the 430-Main Unit and chassis ground.
- ❑ Tune the transceiver and RF signal generator to the center of the UHF band. Modulate the RF signal generator with ±3.5 kHz deviation of a 1 kHz tone.
- ❑ Adjust **T2004** on the 430-Main Unit for maximum voltage on the voltmeter.
- ❑ Confirm -8 dBμ or better 12 dB SINAD at the high and low band edges.

VHF Squelch Preset

❑ Tune to the center of the VHF band, and inject -15 dBμ RF modulated with ±3.5 kHz deviation of a 1 kHz tone to the antenna connector.

❑ Set the **SQL** control to the 10-o' clock position, and adjust **VR1003** on the 144-Main Unit so the squelch just closes.

UHF Squelch Preset

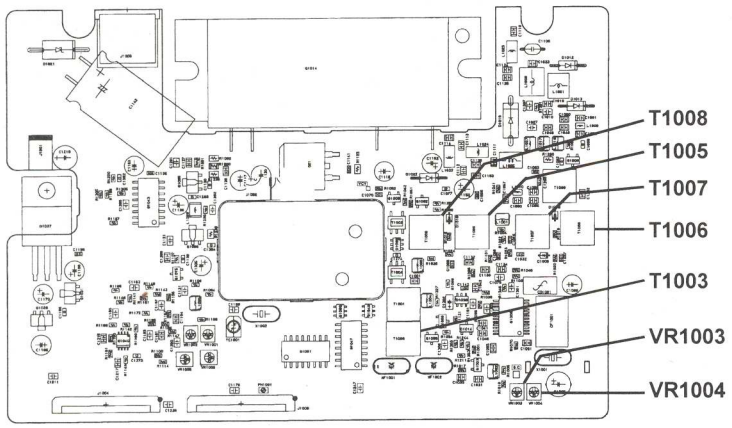
❑ Retune the transceiver and RF signal generator to the center of the UHF band, and with the same injection level and modulation as for VHF, adjust **VR2002** so the squelch just closes.

VHF S-Meter Calibration

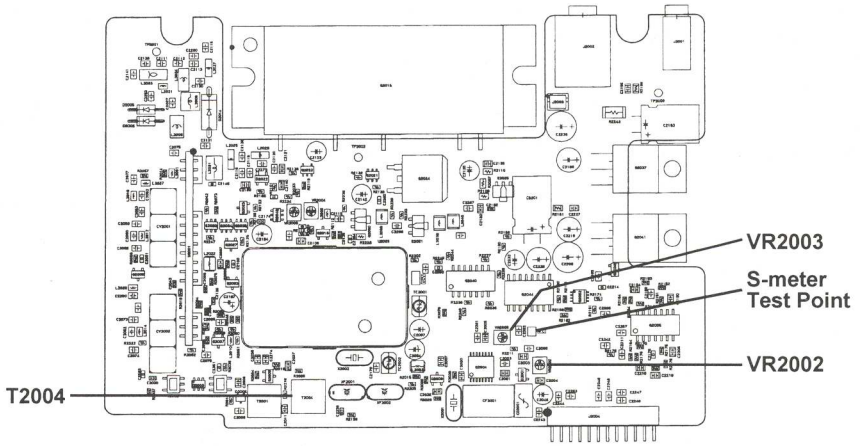
❑ At the center of the VHF band, inject 28 dBμ RF modulated with ±3.5 kHz deviation of a 1 kHz tone to the antenna connector. Adjust **VR1004** on the 144-Main Unit so that all S-meter segments are just on.

UHF S-Meter Calibration

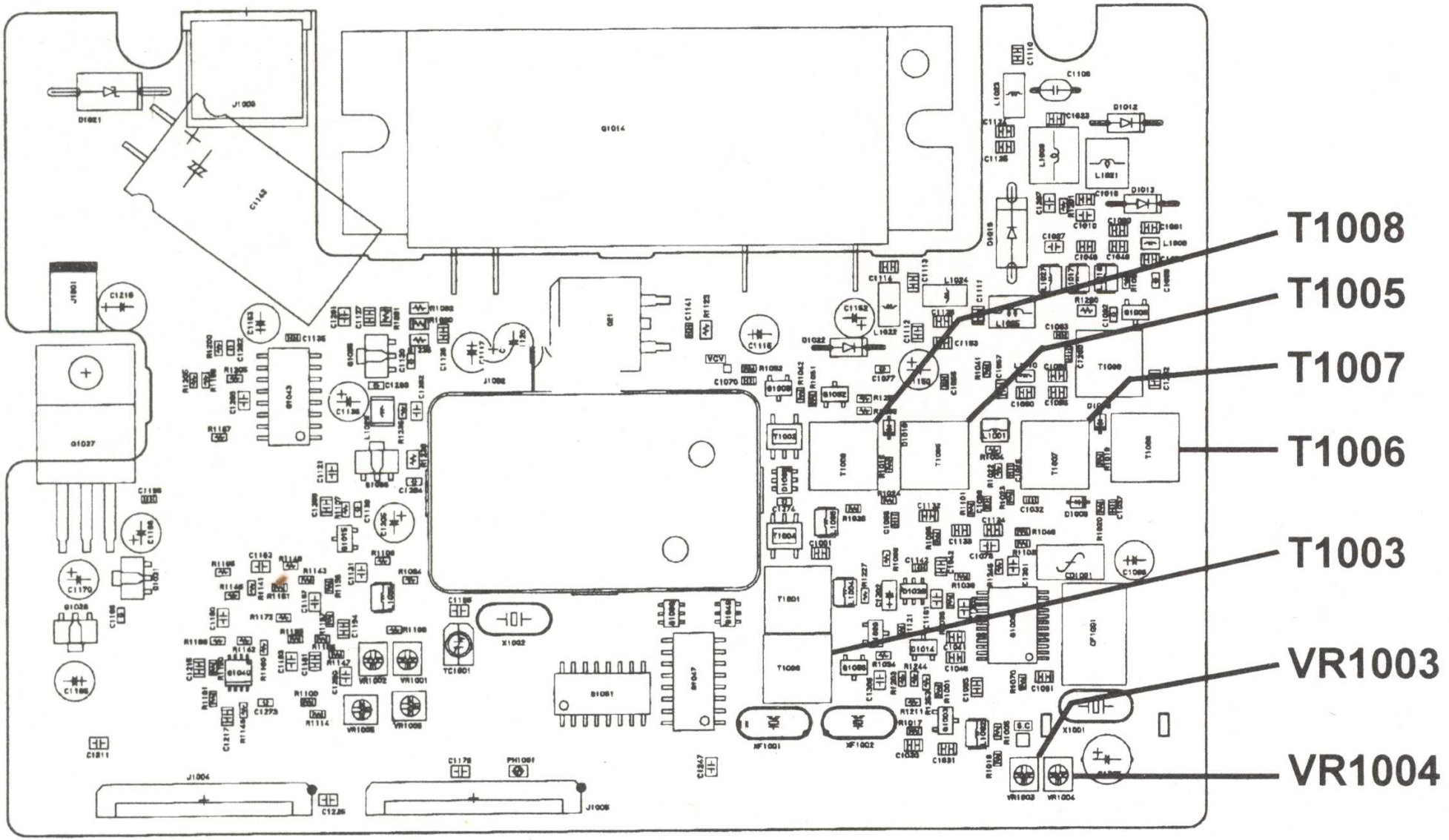
❑ Tune the transceiver and RF signal generator to the center of the UHF band and with the same injection level and modulation, adjust **VR2003** so that all S-meter segments are just on.



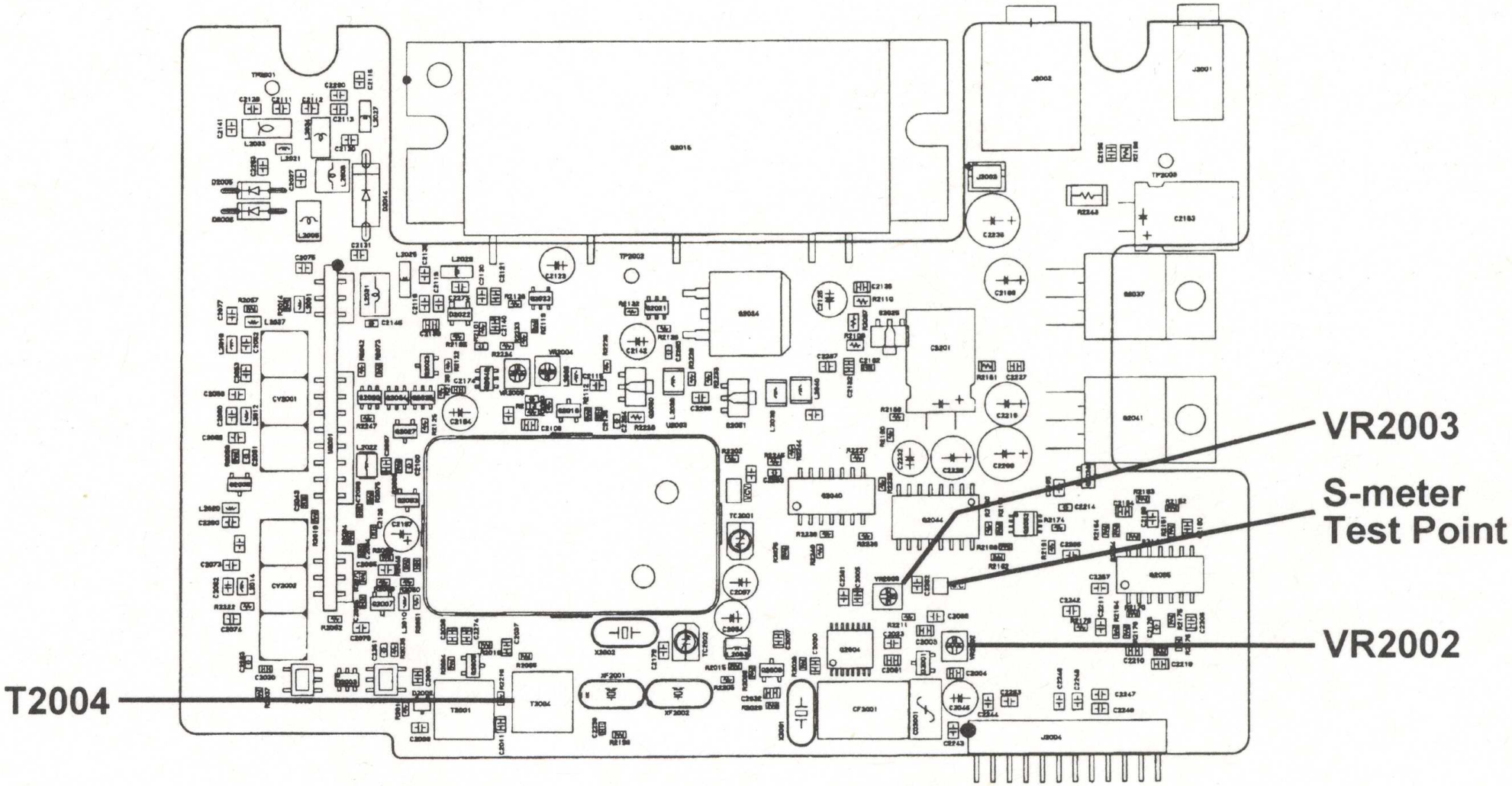
VHF Receiver Alignment Points



UHF Receiver Alignment Points



VHF Receiver Alignment Points



UHF Receiver Alignment Points

The FT-8000R electronics consists of four major boards: the 144 and 430-Main Units, the Panel Unit and the CNTL Unit, and numerous minor boards that mount on these. The Main Unit includes the receiver front ends, IF and PLL subsystem ICs, and support daughter boards for transmit stages, local VCOs, supply regulation and switching circuits, the microprocessors and tone generator/ decoder chips. While reading this description, you can refer to the block diagram for an overview of the major circuit blocks, and to the schematic diagrams for component details.

Antenna Duplexer

Incoming RF from the antenna jack passes through a high-pass and low-pass filter network on the 430-Main Unit before application to two band-switching networks: coil L2031, diode D2014 and capacitors C2146, C2147, C2148, C2152, and resistor R2115 on the 430-Main Unit for UHF signals; and coil L1025, diodes D1012 and D1019 on the 144-Main Unit, and capacitors C2146, C2147, C2148, C2152, resistor R2115 on the 430-Main Unit for VHF signals. These networks filter VHF signals from the UHF receiver and UHF signals from the VHF receiver, allowing each band to operate independently while sharing the same antenna connection.

VHF Reception

VHF signals passed by the duplexer are applied to a varactor-tuned band-pass filter consisting of T1006, T1007, D1001, D1002, D1008 and D1009, after RF amplification by Q1002 (**SGM2016M**). The amplified RF is passed through another RF amplifier Q1001 (**3SK131-V12**), then band-pass filtered again by varactor-tuned resonators T1005, T1008, D1004, D1005, D1010 and D1011 then fed through diode switch D1003 (**DAN235U**) to the Diode Balanced Mixer T1002, T1004 and D1006.

Buffered 155.05 ~ 219.05 MHz output from the 144-VCO Unit is amplified by Q1007 (**2SC3120**) and applied to the 1st mixer. The resulting 45.05-MHz 1st mixer product is passed through monolithic crystal filters XF1001 and XF1002 to strip away all but the desired signal, which is then amplified by Q1003 (**2SC2714Y**) before delivery to FM IF subsystem IC Q1009 (**TK10930V**), containing the 2nd mixer, 2nd local oscillator, limiter amplifier, noise amplifier, S-meter amplifier and squelch gates. A 2nd local signal is generated from 45.505 MHz crystal X1001, which produces the 455 kHz 2nd IF when mixed with the 1st IF signal within Q1009. The 2nd IF is passed through ceramic filter CF1001 to strip away unwanted mixer products, and is then applied to the limiter amp in Q1009, which removes amplitude variations in the 455 kHz IF before detection of the speech by ceramic discriminator CD1001.

VHF Squelch Control

When no carrier is received, noise at the output of the detector stage in Q1009 is amplified and band-pass filtered by the noise amp section of Q1009 and the network between pin 19 and 20, and then rectified by D1014. The resulting DC squelch control voltage is passed to pin 74 of CPU Q3005. While no carrier is received, pin 11 on Q1047 remains low, signaling pin 11 of shift register Q1047 (**μPD4094BG**) which produces the **BUSY** indication on the display when the squelch is open. VHF receiver audio is prevented from signal would be in UHF operation.

VHF AF Output

Detected audio from pin 19 of Q1009 passes through the de-emphasis network consisting of

R1048 & C1078, and high-pass filter consisting of Q1017-2 (**M5223FP**) & associated circuitry and squelch gate, then is applied to pin 11 of Q2044 (**M51132FP**).

Normally, the VHF AF signal appears from pin 10 of Q2044, then passes through AF amplifier Q2035-4 (**NJM2902M**), and low pass filter Q2035-3 to audio amplifier Q2037 (**TDA2003H**). The amplified audio signal is applied to the loudspeaker.

When an external speaker is connected to the **UHF SPKR** jack on the rear panel, the VHF AF signal is applied from pin 7 of Q2052, then passed through AF amplifier Q2035-4, and low-pass filtered by Q2035-3 before application to audio amplifier Q2037 (**TDA2003H**). Amplified audio is delivered via **UHF SPKR** jack to the external speaker.

UHF Reception

The UHF signal is amplified by Q2001 (**SGM2016M**) before it gets to CV2001. It then is amplified by Q2002 (**SGM2016M**) and passes through CV2002 before it gets to diode switch D2004 (**DAN235U**) and is applied to the Diode Balanced Mixer consisting of T2002, T2003 & D2003 (**ND487C1T**).

A local signal generated from the 430-VCO Unit is fed through diode switch D2011 (**DAN235U**) to buffer amplifier Q2007 (**2SC3120**). The buffered local signal then passed through another diode switch D2010 (**DAN235U**), before application to the Diode Balanced Mixer.

The resulting 58.525 MHz 1st IF signal product is passed through monolithic crystal filters XF2001, XF2002 to strip away all but the desired signal, which is then amplified by Q2003 (**2SC2714Y**) before delivery to FM IF subsystem IC Q2004 (**TA31136FN**), which contains the 2nd mixer, 2nd local oscillator, limiter amplifier, noise amplifier, and S-meter amplifier.

A 2nd local signal is generated from 58.07 MHz crystal X2001, to produce the 455 kHz 2nd IF when mixed with the 1st IF signal within Q2004. The 2nd IF passes through ceramic filter CF2001 (**KBF-455R-15A**) to strip away unwanted mixer products, and is then applied to the limiter amp in Q2004, which removes amplitude variations in the 455 kHz IF before detection of speech by ceramic discriminator CD2001 (**CDB455C7**).

UHF Single-Band Dual Receive

When UHF single-band dual receive operation is active, a portion of the received UHF RF passes through high-pass & low-pass filters and antenna switching network before reaching RF amplifier Q2001 (**SGM2016M**). The amplified RF signal is passed through the band-pass filter consisting of C2052, C2053, C2068, C2069, C2077, L2012 & L2018, and is amplified again by Q2006 (**2SC3356-R24**), and is then fed through the diode switch D2007 (**DAN235U**) to the 144-Main Unit.

In the 144-Main Unit, the UHF signal passes through diode switch D1007 (**HSU277**) to the Diode Balanced Mixer consisting of T1002, T1004 & D1006 (**ND487C1T**).

The local signal for sub-receiver generated from the 144-VCO Unit is fed through diode switch D1018 (**DAN235U**) to doubler Q1006 (**2SC3120**). The doubled local signal passes through the high-pass filter consisting of the C1057, C1087 & C1088 and another diode switch D1016 (**DAN235U**) to the Diode Balanced Mixer D1006.

The resulting 45.05 MHz sub receiver 1st IF

signal is received just as a VHF signal would be in VHF operation.

UHF Squelch Control

When no carrier is present, noise at the output of the detector stage in Q2004 is band-pass filtered by the filter amp section of Q2004 and associated circuit. The filtered noise signal is rectified by D2001 (**MA716**), and the resulting DC squelch control voltage is applied on pin 76 of CPU Q3005 (**M37702E6**) on the CNTL Unit.

When a carrier appears at the discriminator, noise is removed from the output, causing pin 6 of Q2039 (**μPD4094BG**) to go low, signaling microprocessor Q3005 to active the SQL gate consisting of Q2040-4 (**μPD4066BG**).

UHF Audio

Detected audio from pin 9 of Q2004 is passed through the de-emphasis circuit consisting of R2012 & C2018, a high-pass filter consisting of Q2009-2 (**M5223FP**) & associated circuit and squelch gate, then is applied to pin 15 of Q2044 (**M51132FP**).

Normally, the UHF AF signal appears from pin 7 of Q2052, and then passes through AF amplifier Q2035-4 (**NJM2902M**), low-pass filter Q2035-3 and on to audio amplifier Q2037 (**TDA2003H**). The amplified audio signal is then applied to the loudspeaker.

When an external speaker is connected to the **UHF SPKR** jack on the rear panel, the UHF AF signal appearing from pin 1 of Q2052 passes through AF amplifier Q2035-1, low-pass filter Q2035-2 and on to audio amplifier Q2041 (**TDA2003H**). The amplified audio signal is delivered via the **UHF SPKR** jack to the external speaker.

Transmit Signal Path

The modulated audio signal originates at the condenser microphone. The AF high frequency component is pre-emphasized by C1179, R1142, R1145, R1160, and Q1032-2 (**NJM2902M**) and amplified by the microphone amplifier circuit. Then, the modulated signal is subjected to amplitude limiting by an IDC (Instantaneous Deviation Control) circuit made up of C1180, R1141, R1146, and Q1032-3 (**NJM2902M**). The signal is buffer amplified C1183, R1148, R1143, R1158, and Q1032-4 (**NJM2902M**), and then passes through a splatter filter consisting of C1181, C1187, C1193, C1194, R1147, R1155, R1156, R1157, R1172, and Q1032-1 (**NJM2902M**). During 145 MHz transmission, the modulated signal is delivered to pin 4 of the 144-VCO Unit. In the case of 435 MHz band transmission, the modulated signal is delivered to pin 11 of electronic volume control Q2044 (**M51132FP**), adjusted to the deviation level which is preset by the CPU, Q3005, exits Q2044 via pin 16, and is then applied to pin 4 of the 430-VCO Unit.

DTMF, Beep, CTCSS tone, or tone burst signals for transmit are generated from the CNTL Unit and applied to the buffer amplifier circuit.

VHF Transmit Signal Path

The modulated signal input to pin 4 of J302 ("**MOD**" terminal) of the 144-VCO Unit frequency-modulates the transmitting VCO made up of D306 (**1SV229**), Q304 (**2SC3356-R24**), etc.

The frequency- modulated signal is buffer-amplified by Q305 (**2SC3356-R24**) and exits from pin 1 of J301 of the 144-VCO Unit. The signal output from pin 1 of J301 of the 144-VCO Unit is buffer-amplified by Q1015 (**2SC3356-R24**) and applied to Q1056 (**2SC3357**) and Q1055 (**2SC2954**).

The signal output from Q1055 is applied for amplification to pin 1 of the Q1014 power mod-

ule (**M67781L**) and exits from pin 4 of the power module. The power module is gain-controlled by the APC circuit.

Power module output passes through a low-pass filter made up of C1109, C1111, C1113, C1114, C1126, L1022, and L1024 to the antenna switch circuit and further to the duplexer circuit, and is delivered to the antenna from the antenna terminal.

VHF Tx APC circuit

A portion of the power module output is rectified by Schottky diode D1022 (**1SS88**), etc. and delivered to the APC circuit made up of Q1023 (**FMS1**), Q1022 (**IMX1**), and Q1021 (**2SA1870E**) as a DC voltage which is proportional to the output level of the power module.

The control data for RF output levels are set by CPU Q3005 (**M37702E6**) on the CNTL Unit. This control data is sent to D/A converter Q1061 (**μPD4094BG**) from which a voltage appropriate to the control data input to Q1023 is derived.

Q1023 (**FMS1**) differentially-amplifies the rectified DC voltage from the power module and the reference voltage from the D/A converter. Q1022 (**IMX1**) converts these into the control voltage for Q1021. The Q1021 (**2SA1870E**) APC control circuit outputs an APC voltage appropriate to the control voltage and varies the APC voltages, thereby controlling transmitter output. It is possible to select "**High**", "**Mid**", or "**Low**" for the transmission output.

If the PLL circuit unlocks during transmission, pin 2 of Q1033 (**SC370651F**) turns '**H**' and an unlock signal is sent from Q1035 (**2SA1586Y**). This unlock signal is applied to Q1022 (**IMX1**) to stop the operation of Q1022 (**IMX1**). At the same time, Q1021 (**2SA1870E**) (APC control circuit) stops operating, causing the APC voltage to become 0 V. Transmission is stopped when the APC voltages of the power module and 144-drive circuit respectively, become 0 V. During reception, a voltage similar to an unlock signal is delivered to Q1022 (**IMX1**) and as the APC voltage of the power module becomes 0 V, transmission is disabled.

UHF Transmission Signal

The modulated signal input to pin 4 of J402 ("**MOD**" terminal) of the 430-VCO Unit frequency modulates the transmitting VCO made up of D406 (**1SV229**), D407 (**1SV230**), Q403 (**2SC3356-R24**), etc.

The signal is buffer-amplified by Q404 (**2SC3356-R24**) and exits from pin 1 of J401 of the 430-VCO Unit.

The signal from pin 1 of the J401 of the 430-VCO Unit is buffer amplified by Q2016 (**2SC3356-R24**) and delivered to the 430-drive circuit.

The signal from the 430-drive circuit is sent for amplification to pin 1 of power module Q2015 (**M57788MR**) and exits from pin 5 of the power module. The power module is gain-controlled by the APC circuit.

The output from the power module passes through a low-pass filter made up of C2121, C2131, C2135, C2275, L2028, and L2029 to the antenna switch circuit, on to the duplexer circuit, and finally to the antenna from the antenna terminal of the 144-Main Unit.

UHF Tx APC circuit

A portion of the output from the power module is rectified by Schottky diode D2022 (**1SS319**), etc. and sent to the APC circuit made up of Q2022 (**FMS1**), Q2021 (**IMX1**), and Q2024 (**2SA1870E**) as a DC voltage which is proportional to the output level of the power module.

The control data for RF output level is preset by CPU Q3005 (**M37702E6**) on the CNTL Unit. This control data is sent to D/A converter Q2039 (**μPD4094BG**), from which a voltage appropriate to the control data value is sent to Q2022 as a reference voltage.

Q2022 (**FMS1**) differentially-amplifies the rectified DC voltage from the power module and the reference voltage from the D/A converter. Q2021 (**IMX1**) converts this difference into the control voltage for Q2014. APC controller Q2024 (**2SA1870E**) outputs an appropriate control voltage and varies the APC voltage at pin 2 of the power module and 430-drive circuit, thereby controlling the RF output level. It is possible to select "**High**", "**Mid**" or "**Low**" for the RF output power levels.

If the PLL circuit unlockes during transmission, pin 2 of Q2032 (**SC370651F**) turns '**H**' and an unlock signal is sent from Q2036 (**2SA1586Y**). This unlock signal is input to Q2021 (**IMX1**) to disable Q2021 (**IMX1**). At the same time, APC controller Q2024 (**2SA1870E**) voltage becomes becomes 0 V, thus disabling transmission from the power module and 430-drive circuit. During reception, a voltage similar to an unlock signal is sent to Q2021 (**IMX1**), and the APC voltages of the power module and 430-drive circuit become 0 V, transmission is disabled.

VHF PLL

The PLL circuit consists of PLL subsystem IC Q1033 (**SC370651F**), which includes a comparative frequency divider, reference frequency divider, phase comparator, charge pump, shift register, latch, etc.

The output from pin 1 of J301 of the 144-VCO Unit is divided by the comparative frequency divider according to the frequency dividing data that is associated with the setting frequency input from the CPU. It is then sent to the phase comparator.

The 12.8 MHz frequency of the reference oscillator circuit made up of X1002 and Q1029 (**2SC2812-L6**) is divided by the reference frequency divider into 2,560 or 2,048 parts to become 5 kHz or 6.25 kHz comparative reference frequencies, which are utilized by the phase comparator. Either of the comparative reference frequencies is selected according to frequency steps: 5 kHz is selected for the 5/ 10/ 15/ 20 kHz steps, and 6.25 kHz is selected for the 12.5/ 25/ 50 kHz steps.

The phase comparator compares the phase between the frequency-divided oscillation frequency of the VCO circuit and comparative reference frequency (5 kHz or 6.25 kHz) and outputs a pulse corresponding to the phase difference. This pulse is integrated by the charge pump and loop filter into a control voltage (**VCV**) to control the oscillation frequency of the VCO circuit.

When the power is turned on or the tx/rx operation is switched, the frequency and the frequency dividing ratio data for the reference frequency divider are serially transmitted from the CPU to the divider. This serial data is converted by the shift register and latch into parallel data to control the reference frequency divider and comparative frequency divider.

The presence or absence of phase difference as the result of comparison by the phase comparator is sent as an "**Unlock**" signal from the lock detector circuit inside the PLL IC. This signal is sent to the APC circuit to disable transmission when the PLL circuit is unlocked.

UHF PLL

The PLL circuit consists of PLL subsystem IC Q2032 (**SC370651F**), which includes a comparative frequency divider, reference frequency divider, phase comparator, charge pump, shift register, latch, etc.

The output from pin 1 of J401 of the 430-VCO Unit is divided by the comparative frequency divider according to the frequency dividing data that is associated with the setting frequency input from the CPU. It is then sent to the phase comparator.

The 12.8 MHz frequency of the reference oscillator circuit made up of X2002 and Q2029 (**2SC2812-L6**) is divided by the reference frequency divider into 2,560 or 2,048 parts to become 5 kHz or 6.25 kHz comparative reference frequencies, which are utilized by the phase comparator. Either of the comparative reference frequencies is selected according to frequency steps: 5 kHz is selected for the 10/ 20 kHz steps, and 6.25 kHz is selected for the 12.5/ 25/ 50 kHz steps.

The phase comparator compares the phase between the frequency-divided oscillation frequency of the VCO circuit and comparative reference frequency (5 kHz or 6.25 kHz) and outputs a pulse corresponding to the phase difference. This pulse is integrated by the charge pump and loop filter into a control voltage (**VCV**) to control the oscillation frequency of the VCO circuit.

When the power is turned on or the tx/rx operation is switched, the frequency and the frequency dividing ratio data for the reference frequency divider are sent serially from the CPU to the PLL IC. This serial data is converted by the shift register and latch into parallel data to control the reference frequency divider and comparative frequency divider.

The presence or absence of phase difference as the result of comparison by the phase comparator is send as an "**Unlock**" signal from the lock detector circuit inside the PLL IC. This signal is sent to the APC circuit to disable transmission when the PLL circuit is unlocked.

DC 13.8V
FUSE
T9206228
GND
13.8V
SP0001
SP
T9206438
J1001
SP
GND

144-MAIN-UNIT
F3599000

J1003
DATA
SQC
PK1200
PK9600
PKS
GND
PKD

144-VCO-UNIT
F3603101
1 GND
2 VCV
3 GND
4 MOD
OUT 5
GND 6
GND 7
9V 8
TRX 9

ANT
13.8V
SP

430-VCO-UNIT
F3603102
5 OUT
6 GND
7 TX
8 9V
9 RX
GND 1
VCV 2
GND 3
MOD 4

430-MAIN-UNIT
F3600101

FN0001
FAN
J2003
FAN 1
GND 2

J2002
UHF-SP

J2001
EXT-SP

T9206516 (DST USA)
T9206005 (DST EXP)
ANT
P0003
ANT

J1005
1 V&V
2 GND
3 GND
4 U&U
5 GND
6 HEAT
7 U MOD
8 GND
9 MIC
10 GND
11 BEEP
12 GND
13 V DET
14 V MTR
15 V NOISE
16 V AF
17 GND
18 V UNLOCK

J1004
1 GND
2 V CLOCK
3 V DATA
4 V STB1
5 V STB2
6 V STB3
7 GND
8 POWER ON
9 GND
10 PKS
11 U PK9600
12 U PK1200
13 GND
14 U SQL SW
15 GND
16 9V
17 9V
18 13.8V

PB3001
F3298000
FPC

1 V&V
2 GND
3 GND
4 U&U
5 GND
6 HEAT
7 U MOD
8 GND
9 MIC
10 GND
11 BEEP
12 GND
13 V DET
14 V MTR
15 V NOISE
16 V AF
17 GND
18 V UNLOCK
19 GND
20 V CLOCK
21 V DATA
22 V STB1
23 V STB2
24 V STB3
25 GND
26 POWER ON
27 GND
28 PKS
29 U PK9600
30 U PK1200
31 GND
32 U SQL SW
33 GND
34 9V
35 9V
36 13.8V

J2004
1 U&U
2 GND
3 V&V
4 V VOL
5 U MOD
6 U PK9600
7 U MTR
8 V AF
9 U PK1200
10 U NOISE
11 U STB1
12 FAN CNTL
13 U DATA
14 U STB2
15 U VOL
16 U CLOCK
17 BEEP
18 9V
19 U UNLOCK
20 GND
21 U SQL SW
22 NC
23 U DET
24 MUTE

J3007
1 U&U
2 GND
3 V&V
4 V VOL
5 U MOD
6 U PK9600
7 U MTR
8 V AF
9 U PK1200
10 U NOISE
11 U STB1
12 FAN CNTL
13 U DATA
14 U STB2
15 U VOL
16 U CLOCK
17 BEEP
18 9V
19 U UNLOCK
20 GND
21 U SQL SW
22 NC
23 U DET
24 MUTE

CNTL-UNIT
F3062101

MIC
J3003
1 NC
2 NC
3 9V
4 9V
5 MIC
6 ACC

J3006
1 TONE
2 5V
3 V IN
4 NC
5 U IN
6 V DET
7 U DET
8 GND
9 TSQ V STB
10 TSQ U STB
11 TSQ DATA
12 TSQ CLOCK

1 TONE
2 5V
3 A IN
4 TCHK
5 B IN
6 A DET
7 B DET
8 GND
9 A STB
10 B STB
11 DATA
12 CLOCK

TONE-SQL-UNIT
FTS-22 (OPTION)

J3001
1 U RX LED
2 U TX LED
3 U SQL
4 U VOL
5 GND
6 CE2
7 LCD CLOCK
8 LCD DATA
9 CE1
10 INH
11 5V
12 DIM CNTL
13 GND
14 POWRE SW
15 KEY STB2
16 KEY STB1
17 D7
18 D6
19 D5
20 D4
21 D3
22 D2
23 D1
24 D0
25 V RX LED
26 V TX LED
27 V SQL
28 V VOL
29 CK B
30 CK A

T9206568

J4001
1 U RX LED
2 U TX LED
3 U SQL
4 U VOL
5 GND
6 CE2
7 LCD CLOCK
8 LCD DATA
9 CE1
10 INH
11 5V
12 DIM CNTL
13 GND
14 POWER SW
15 KEY STB2
16 KEY STB1
17 D7
18 D6
19 D5
20 D4
21 D3
22 D2
23 D1
24 D0
25 V RX LED
26 V TXN LED
27 V SQL
28 V VOL
29 CK B
30 CK A

PANEL-UNIT
F3601101

VR-L-UNIT
F3598101A

KEY STB2 1
V VOL 2
GND 3
BAND A 4
V SQL 5
5V 6
J501

1 KEY STB2
2 V VOL
3 GND
4 BAND A
5 V SQL
6 5V
J4002

VR-R-UNIT
F3598102A

U SQL 1
KEY STB2 2
GND 3
U VOL 4
5V 5
BAND B 6
J4003

1 U SQL
2 KEY STB2
3 GND
4 U VOL
5 5V
6 BAND B
J601

BLOCK

144-MAIN-UNIT F3599000

144-VCO-UNIT F3603101

CNTL-UNIT F3062101

OPTION

TONE SQL-UNIT FTS-22

430-MAIN-UNIT F3600101

430-VCO-UNIT F3603102

PANEL-UNIT F3601101

VR-L-UNIT F3598101A

VR-R-UNIT F3598102A

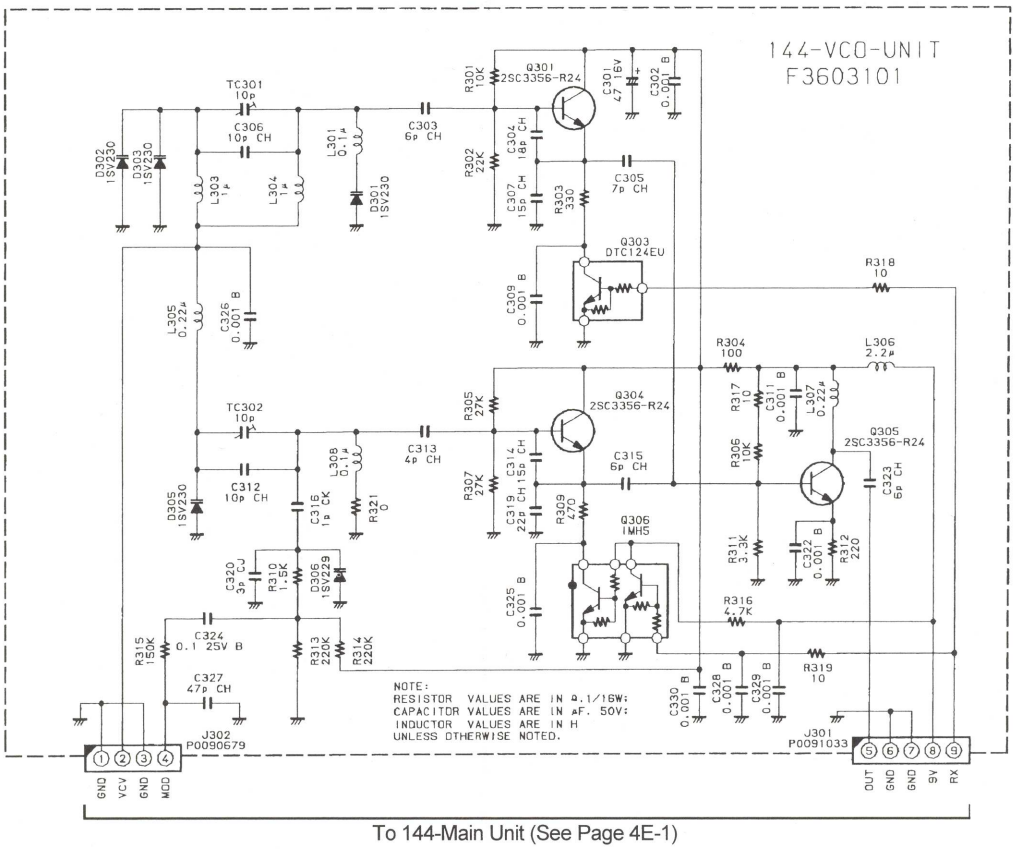
KEY MATRIX

$F_{TX} = 144 \sim 148$ MHz
$F_{RX} = 430 \sim 440$ MHz
$F_{IF} = 45.090$ MHz
$F_{LO1} = F_{RX} + F_{IF}$
$F_{LO2} = F_{RX} + F_{IF}$
$F_{LO3} = (F_{LO1} - F_{LO2})/2$

$F_{TX} = 144 \sim 148$ MHz
$F_{RX} = 430 \sim 440$ MHz
$F_{LO1} = 56.525$ MHz
$F_{LO2} = F_{RX} + F_{IF}$
$F_{LO3} = (F_{LO1} - F_{LO2})/2$
$F_{VCO} = F_{TX}$

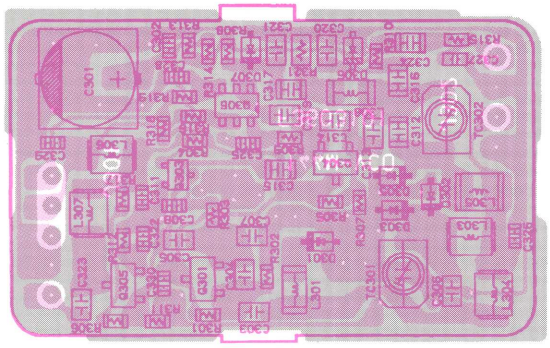
RX LINE
TX LINE
COMMON LINE

Circuit Diagram

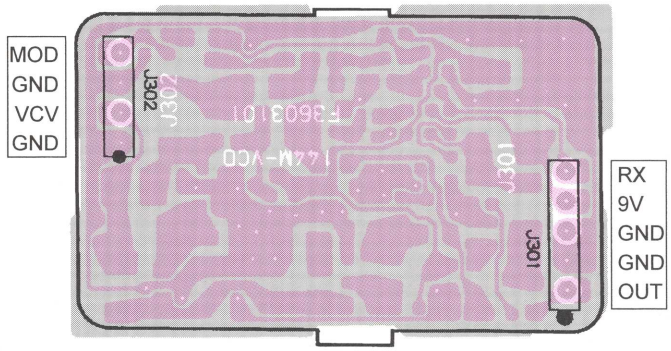


To 144-Main Unit (See Page 4E-1)

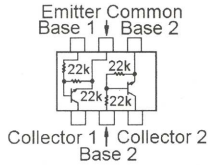
Parts Layout



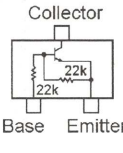
obverse view of component side



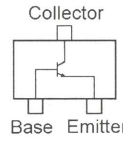
obverse view of connector side



IMH5 (H5)
(Q306)

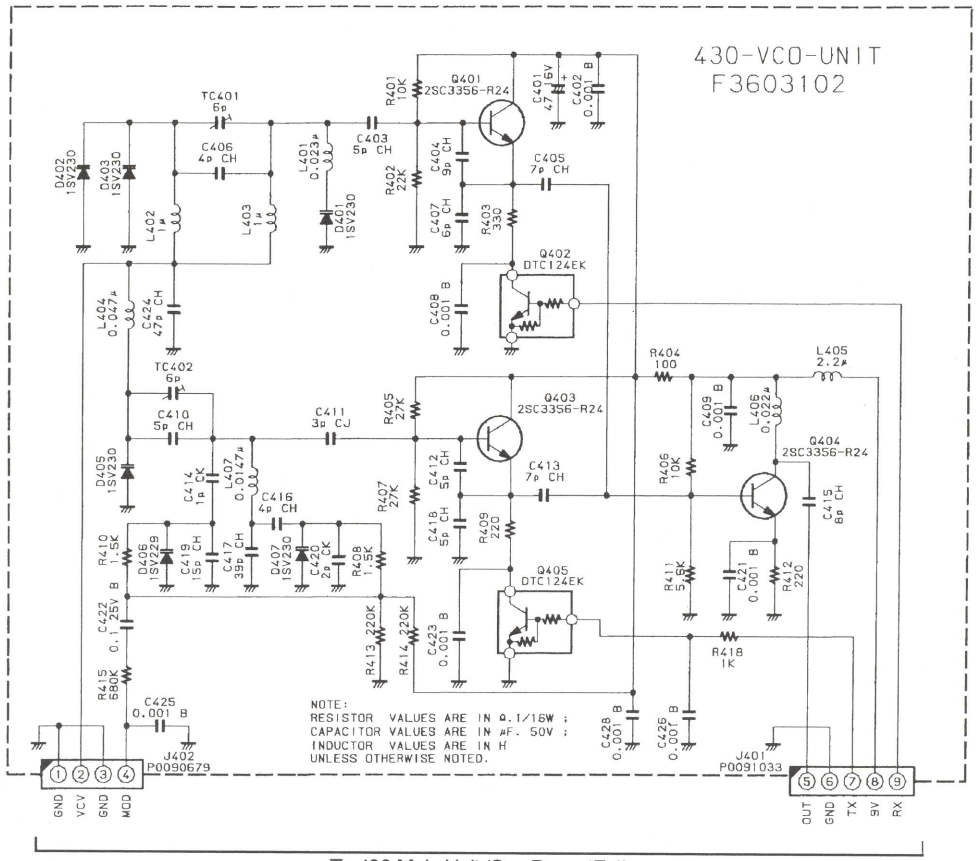


DTC124EU (25)
(Q303)



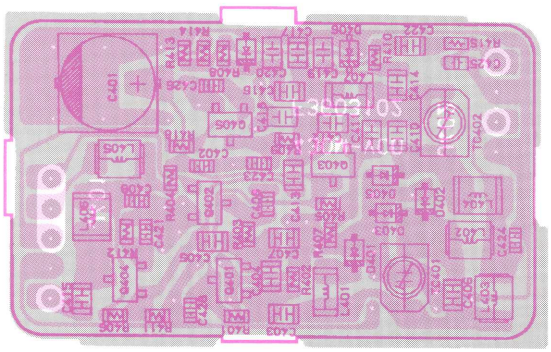
2SC3356 (R24)
(Q301,304,305)

Circuit Diagram

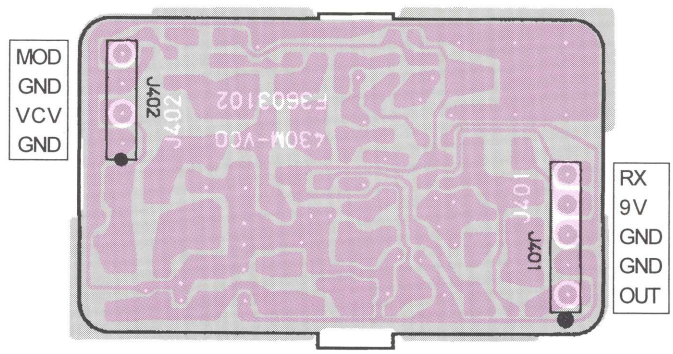


To 430-Main Unit (See Page 4F-1)

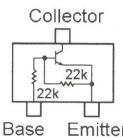
Parts Layout



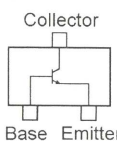
obverse view of chip side



obverse view of connector side

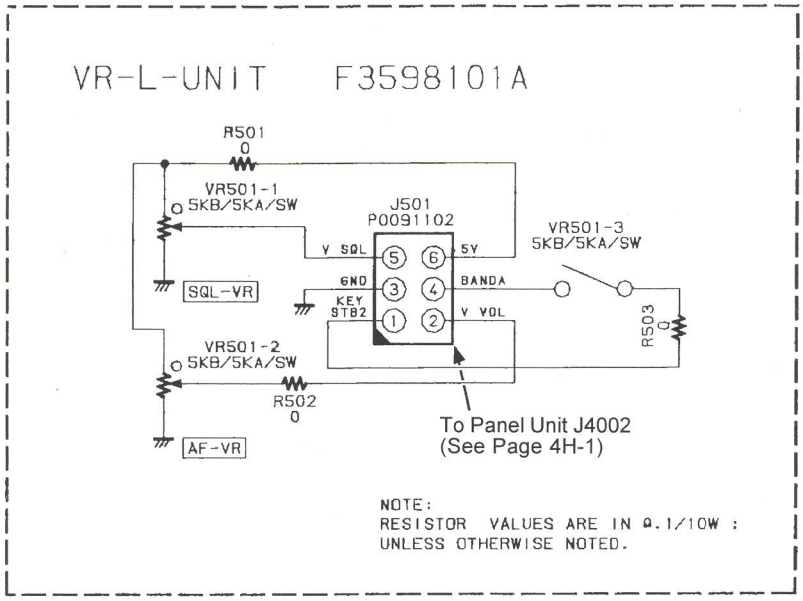


DTC124EK (25)
(Q402,405)

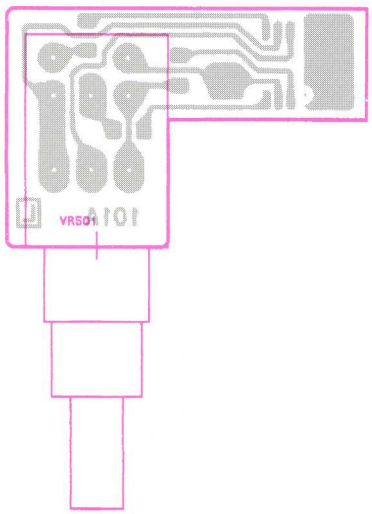


2SC3356 (R24)
(Q401,403,404)

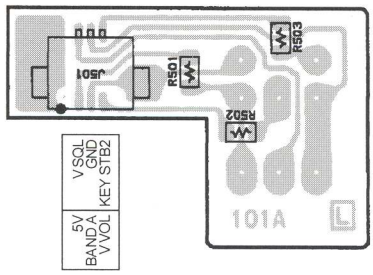
Circuit Diagram



Parts Layout



obverse view of component side

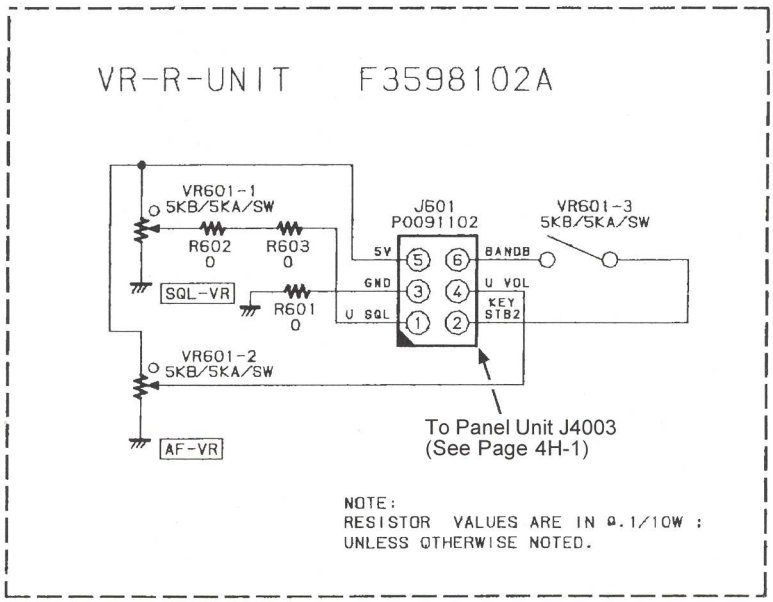


obverse view of connector side

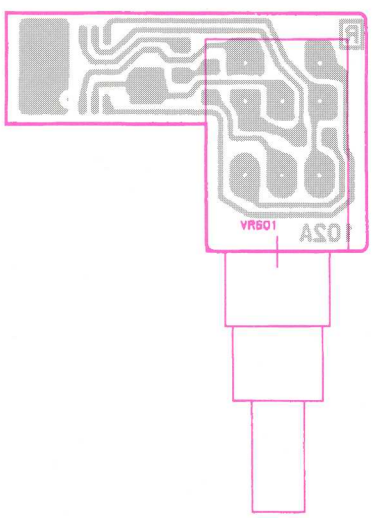
Parts List

REF.	DESCRIPTION	VALUE	WV	TOL.	MFGR'S DESIG	YAESU P/N	VERS.	LOT.	LAY ADR
		*** VR-L UNIT ***							
	PCB with Components					CA1599001			
	Printed Circuit Board					F3598101A			
J 0501	CONNECTOR				IL-WX-6PB-HF-HD-S-B-E1000	P0091102			
R 0501	CHIPRES.	0	1/10W	5%	RMC1/10T 000J	J24205000			
R 0502	CHIPRES.	0	1/10W	5%	RMC1/10T 000J	J24205000			
R 0503	CHIPRES.	0	1/10W	5%	RMC1/10T 000J	J24205000			
VR0501	POT.	5KB/5KA/SW			TP96D00A17.5FB5KX2	J62800118			

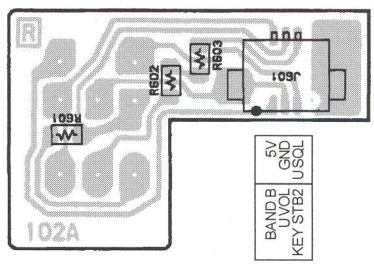
Circuit Diagram



Parts Layout



obverse view of component side

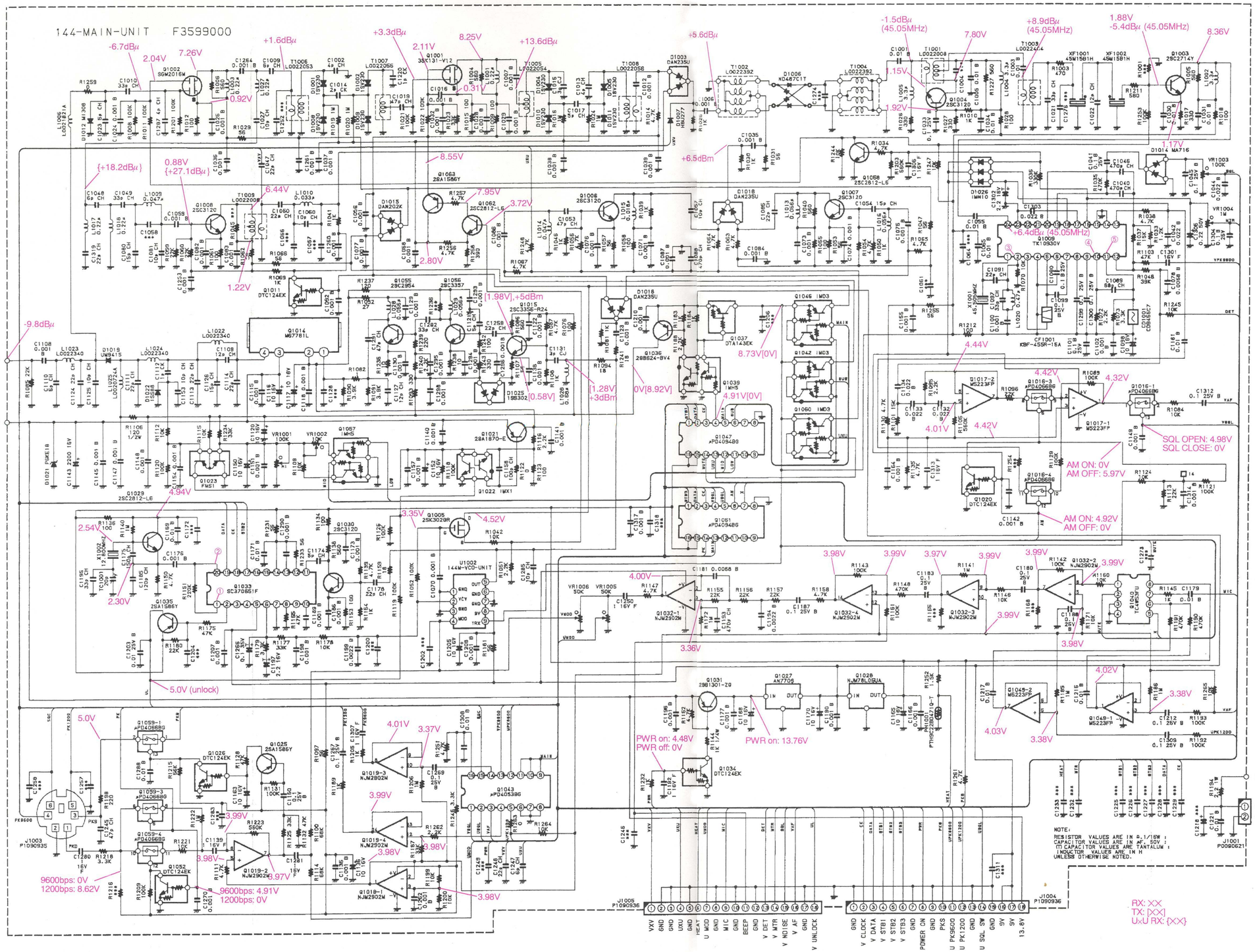


obverse view of connector side

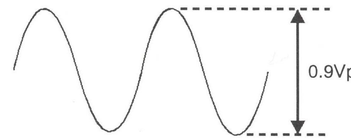
Parts List

REF.	DESCRIPTION	VALUE	WV	TOL	MFGR'S DESIG	YAESU P/N	VERS.	LOT.	LAY ADR
		*** VR-R UNIT ***							
	PCB with Components					CP5613001			
	Printed Circuit Board					F3598101A			
J 0601	CONNECTOR				IL-WX-6PB-HF-HD-S-B-E1000	P0091102			
R 0601	CHIPRES.	0	1/10W	5%	RMC1/10T 000J	J24205000			
R 0602	CHIPRES.	0	1/10W	5%	RMC1/10T 000J	J24205000			
R 0603	CHIPRES.	0	1/10W	5%	RMC1/10T 000J	J24205000			
VR0601	POT.	5KB/5KA/SW			TP96D00A17.5FB5KX2	J62800118			

Circuit Diagram



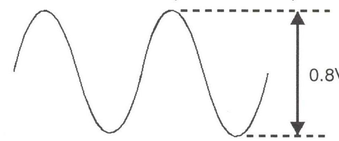
① Q1033 Pin 1 (12.8MHz)



② Q1033 Pin 20 (12.8MHz)



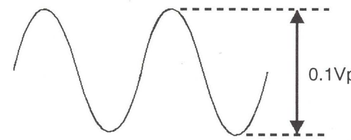
③ Q1009 Pin 2 (45.505MHz)



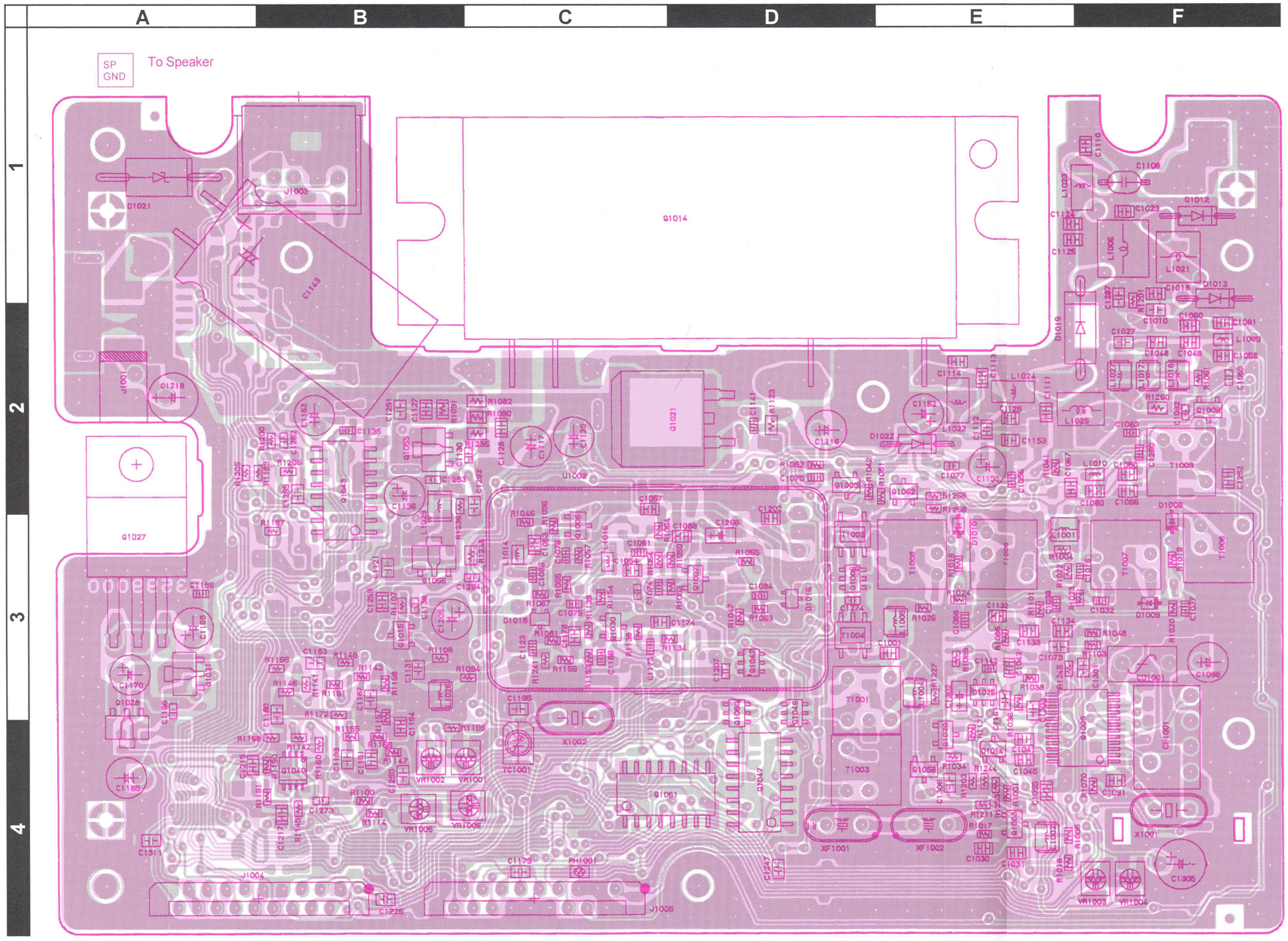
④ Q1009 Pin 10 (455kHz)

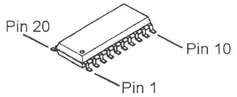


⑤ Q1009 Pin 11 (455kHz)

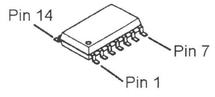


Parts Layout

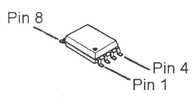




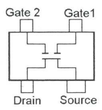
SC370651FR
(Q1033)



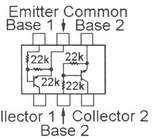
NJM2902M
(Q1019,1032)
µPD4066BG
(Q1016,1059)



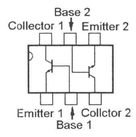
M5223FP
(Q1017,1049)



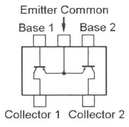
SGM2016M (M-)
(Q1002)
3SK131 (V12)
(Q1001)



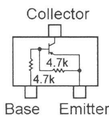
IMH5 (H5)
(Q1039,1057)



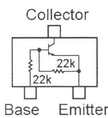
IMX1 (X1)
(Q1022)



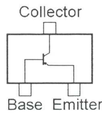
FMS1 (S1)
(Q1023)



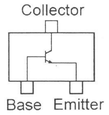
DTA143EK (13)
(Q1037)



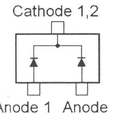
DTC124EK (25)
(Q1011,1026,
1034,1052)



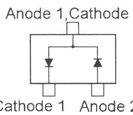
2SA1586Y (SY)
(Q1025,1035,1063)
2SB624 (BV3)
(Q1036)



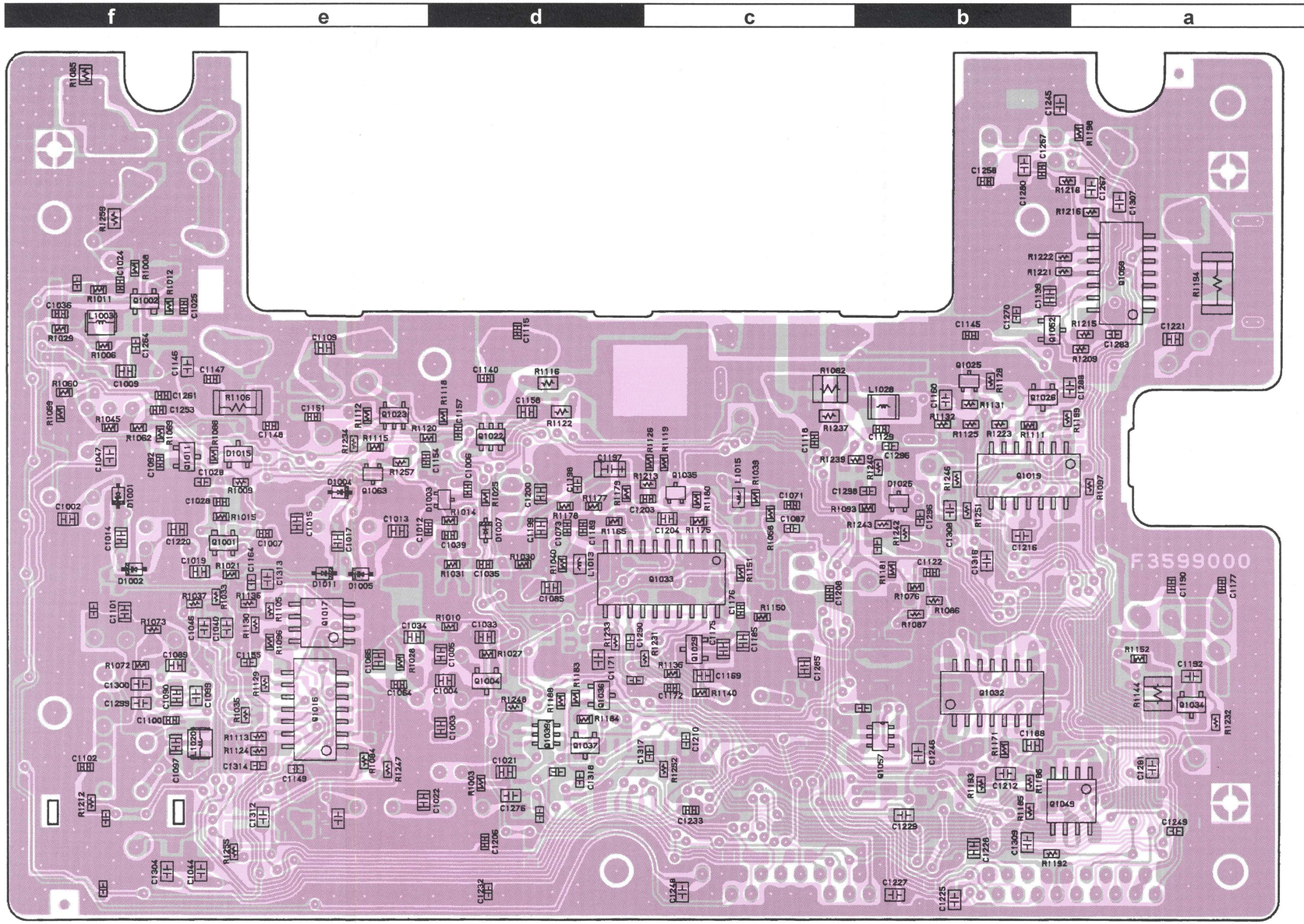
2SC2812 (L6)
(Q1029)
2SC3120 (HB)
(Q1004)



DAN235U (M)
(D1003)
DAN202K (N)
(D1015)

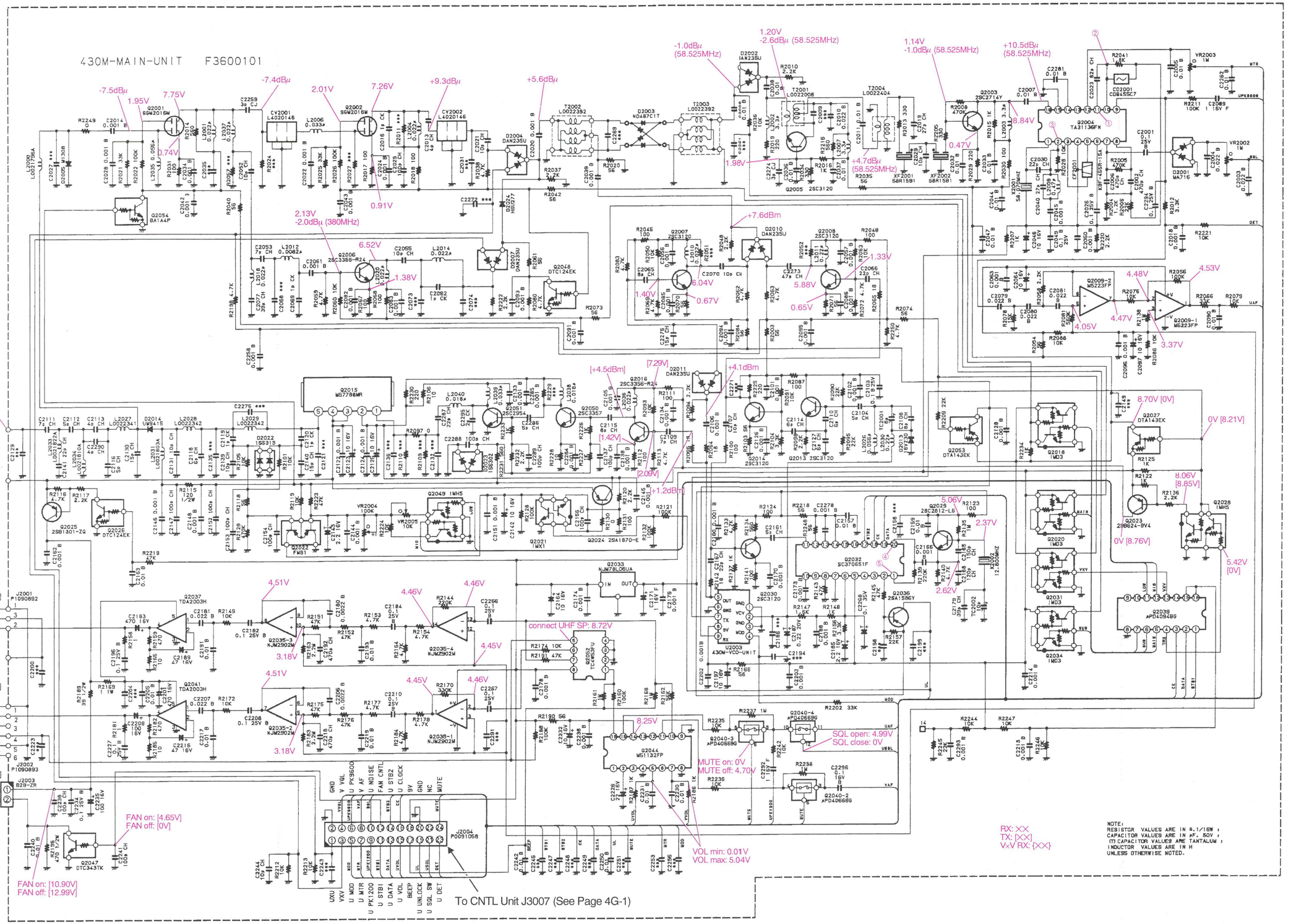


1SS302 (C3)
(D1025)

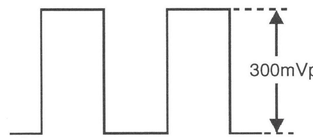


obverse view of chip side

Circuit Diagram



① Q2004 Pin 11 (455kHz)



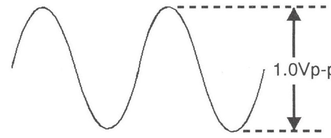
② Q2004 Pin 10 (455kHz)



③ Q2004 Pin 2 (58.070MHz)



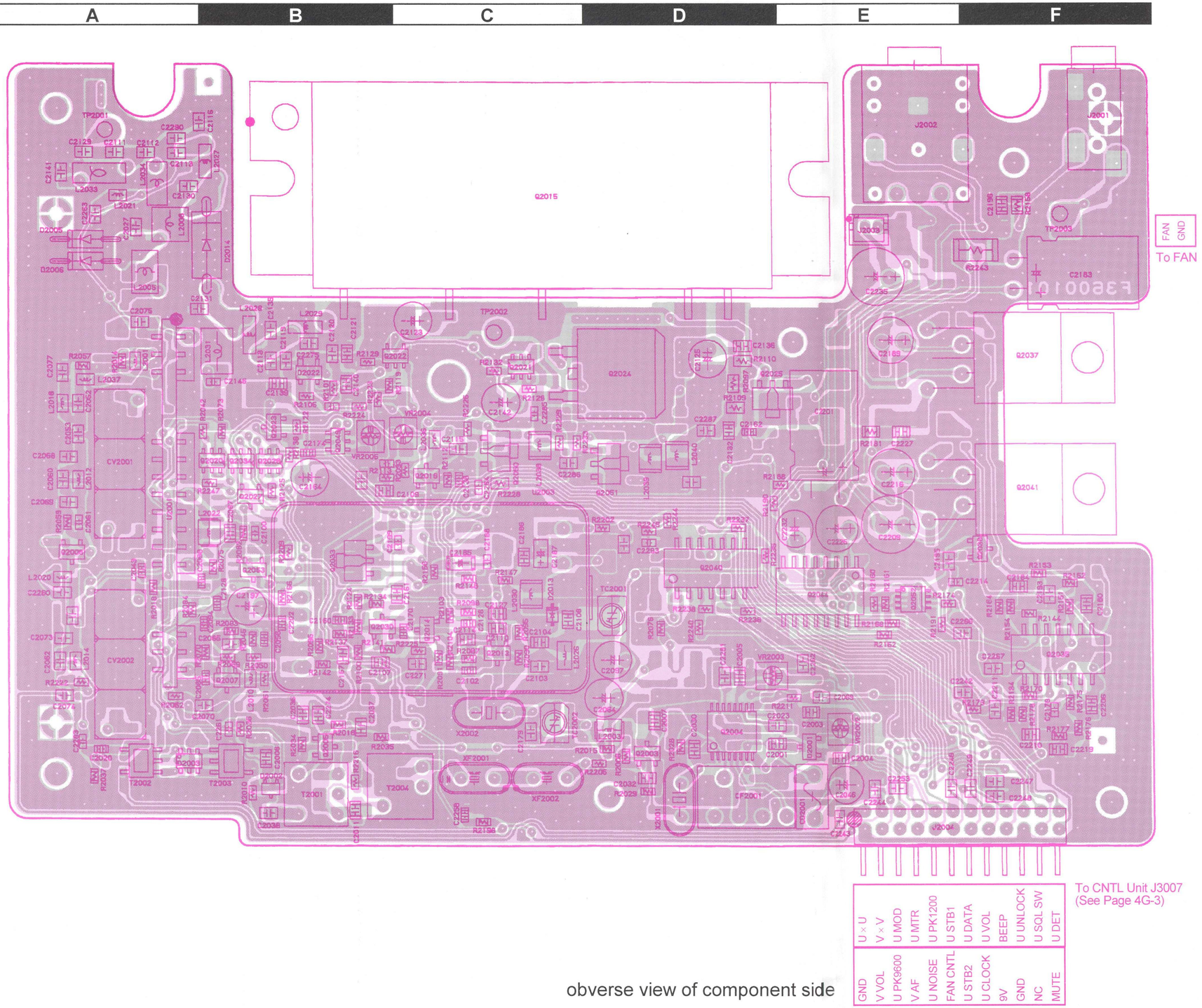
④ Q2032 Pin 20 (12.8MHz)



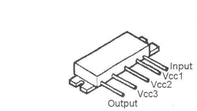
⑤ Q2032 Pin 1 (12.8MHz)



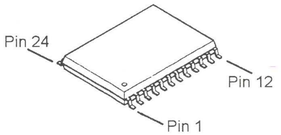
Parts Layout



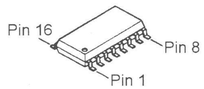
obverse view of component side



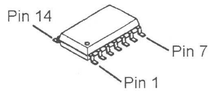
M57788MR
(Q2015)



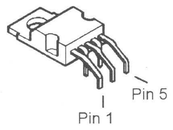
TA31136FN
(Q2004)



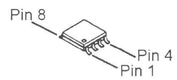
M51132FP
(Q2044)



NJM2902M
(Q2035)
µPD4066BG
(Q2040)



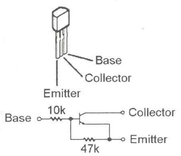
TDA2003H
(Q2037,2041)



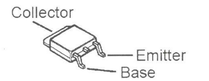
TC4W53FU
(Q2052)



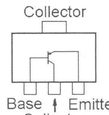
NJM78L05UA (8C)
(Q2033)



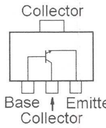
BA1A4P
(Q2054)



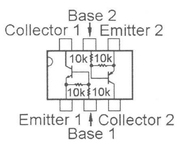
2SA1870
(Q2024)



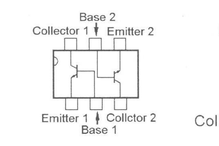
2SB1301
(Q2025)



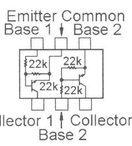
2SC2954 (QK)
(Q2051)
2SC3357 (RK)
(Q2050)



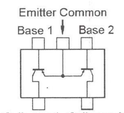
IMD3 (D3)
(Q2020,2034)



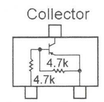
IMX1 (X1)
(Q2021)



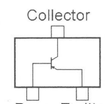
IMH5 (H5)
(Q2028,2049)



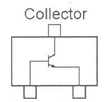
FMS1 (S1)
(Q2022)



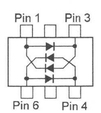
DTA143EK (13)
(Q2027,2053)



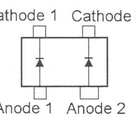
2SB624 (BV3)
(Q2023)



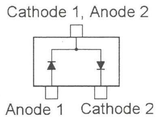
2SC2714Y (QY)
(Q2003)
2SC3120 (HB)
(Q2005,2007,2013,
2014,2030)
2SC3356 (R24)
(Q2006,2016)



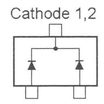
ND487C1T (T1A)
(D2003)



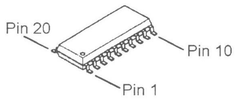
1SS319 (A4)
(D2022)



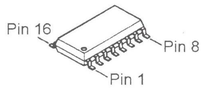
MA716 (M1U)
(D2001)



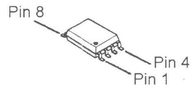
DAN235U (M)
(D2002)



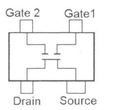
SC370651FR
(Q2032)



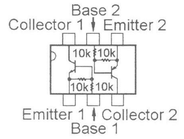
µPD4094BG
(Q2039)



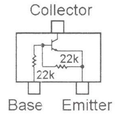
M5223FP
(Q2009)



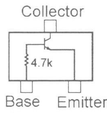
SGM2016M (M-)
(Q2001,2002)



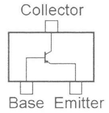
IMD3 (D3)
(Q2018,2031)



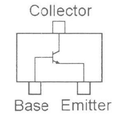
DTC124EK (25)
(Q2026,2048)



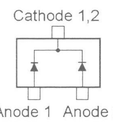
DTC343TK (H03)
(Q2047)



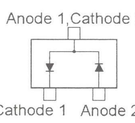
2SA1586Y (SY)
(Q2036)



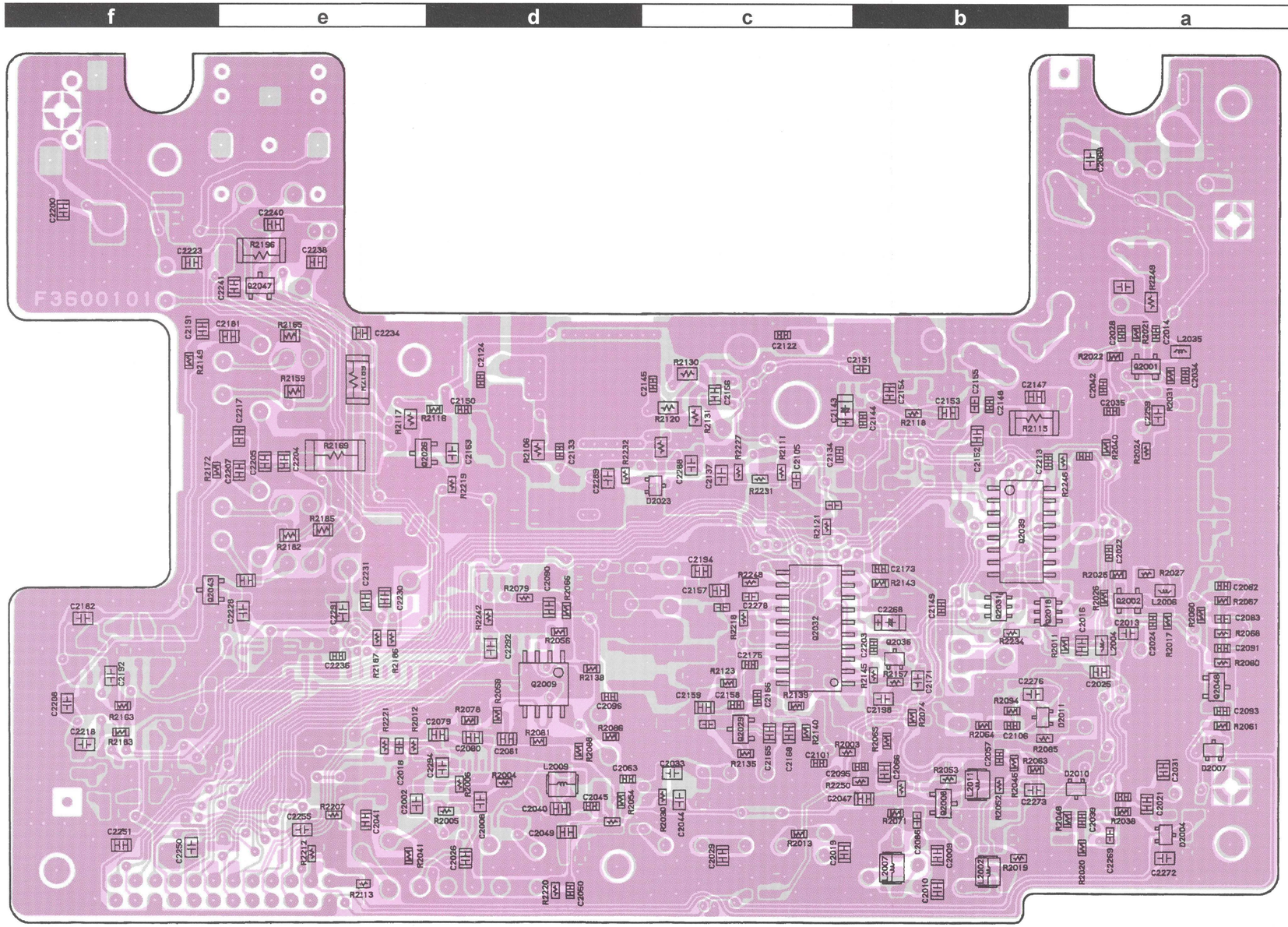
2SC2812 (L6)
(Q2029)
2SC3120 (HB)
(D2008)



DAN235U (M)
(D2004,2007,2010,2011)



1SS302 (C3)
(D2023)



obverse view of chip side

Circuit Diagram

CNTL-UNIT F3062101

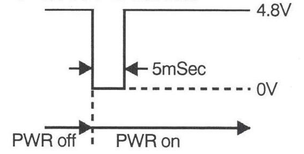
NOTE:
RESISTOR VALUES ARE IN Ω. 1/16W :
CAPACITOR VALUES ARE IN μF. 50V :
(T) CAPACITOR VALUES ARE TANTALUM :
UNLESS OTHERWISE NOTED.

Q3005 M37702E6BFP

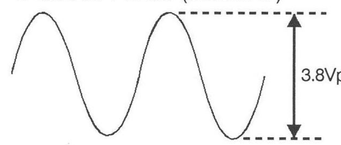
Q3002 2SA1179-M6 · Q3001 DTC144EK · Q3003 M51951AML · Q3004 NJM78L05UA · Q3010 NJM78L05UA · Q3006 IMH5 · Q3007 IMD3 · Q3008-1 NJM2902M · Q3008-2 NJM2902M · Q3008-3 NJM2902M · Q3008-4 NJM2902M · Q3012-1 NJM2902M · Q3012-2 NJM2902M · Q3012-3 NJM2902M · Q3012-4 NJM2902M · Q3002 2SB1182F5-Q · Q3011 2SC2812-L6 · D3001 · D3002 FMN1 · D3003 1SS319 · D3004 FMN1 · D3005 FMN1 · D3006 FMN1 · D3007 1M03 · D3008 · D3009 DAP202U · BT3001 CR2016-TS1 · X3001 8.00MHz

5.04V · PWR on: 4.67V PWR off: 0V · 4.72Vp-p · 2.49V · 2.47V · 2.44V · 3.25V · 3.04V · 2.60V · DIM: 0.56V~3.98V · DIM: 0.1V~8.55V

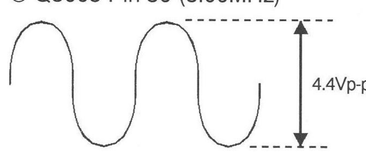
① Q3001 Collector



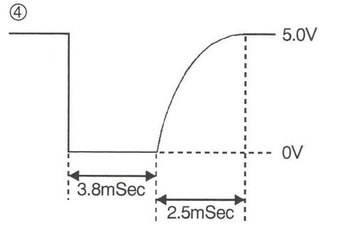
② Q3005 Pin 29 (8.00MHz)



③ Q3005 Pin 30 (8.00MHz)



④



To Panel Unit J4001
(See Page 4H-1)

To Microphone
(See Page 5B-1,5C-1)

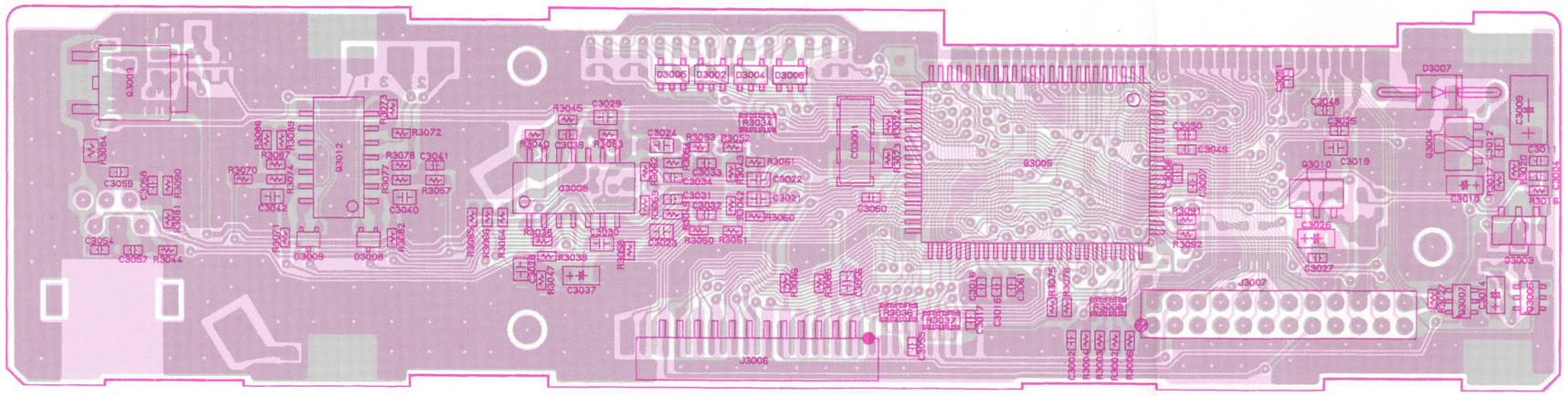
To 430-Main Unit J2004
(See Page 4F-1)

KEY LOCK & Press MHz Key : 2.85Vp-p

To 144-Main Unit J1004,1005
(See Page 4E-1)

To FTS-22 Tone Squelch Unit
(See Page 5A-1)

Parts Layout



J3005
TSQ CLOCK
TSQ DATA
TSQ U STB
TSQ V STB
GND
U DET
V DET
U IN
NC
V IN
5V
TONE

To FTS-22 Tone Squelch Unit
(See Page 5A-1)

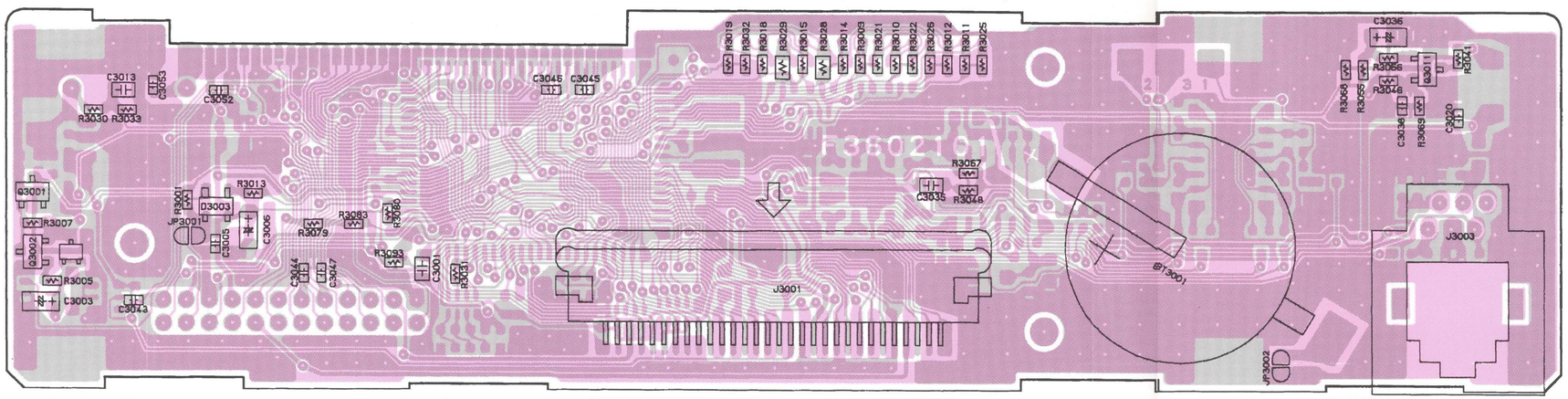
J3007												
U-U	V-V	U MOD	U MTR	U PK1200	U STB1	U DATA	U VOL	BEEP	U UNLOCK	U SQL SW	U DET	
GND	V VOL	U PK9600	V AF	U NOISE	FAN CNTL	U STB2	CLOCK	9V	GND	SP	MUTE	

To 430-Main Unit J2004
(See Page 4F-3)

obverse view of CPU side

To 144-Main Unit J1004,1005
(See Page 4E-3)

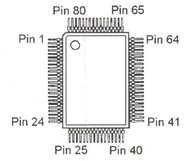
J3001
36. 13.8V
35. 9V
34. 9V
33. GND
32. U SQL SW
31. GND
30. U PK1200
29. U PK9600
28. PKS
27. GND
26. POWER ON
25. GND
24. V STB2
23. V STB1
22. V DATA
21. V CLOCK
20. V UNLOCK
19. GND
18. V AF
17. GND
16. V NOISE
15. V METER
14. V DET
13. GND
12. BEEP
11. GND
10. MIC
9. GND
8. U MOD
7. HEAT
6. GND
5. U U
4. GND
3. GND
2. GND
1. V-V



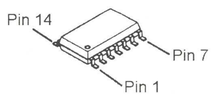
J3001
CK A
CK B
V VOL
V SQL
V TX LED
V RX LED
D0
D1
D2
D3
D4
D5
D6
D7
KEY STB1
KEY STB2
POWER SW
GND
DIM CNTL
5V
INH
CE1
LCD DATA
LCD CLOCK
CE2
GND
U VOL
U SQL
U TX LED
U RX LED

To Panel Unit J4001
(See Page 4H-3)

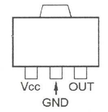
obverse view of connector side



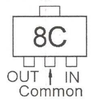
M37702E6BFP
(Q3005)



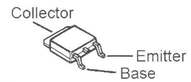
NJM2902M
(Q3008,3012)



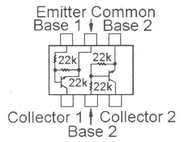
M51951AML (51)
(Q3003)



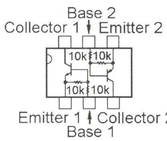
NJM78L05UA (8C)
(Q3004,3010)



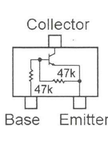
2SB1182
(Q3009)



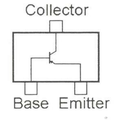
IMH5 (H5)
(Q3006)



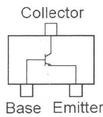
IMD3 (D3)
(Q3007)



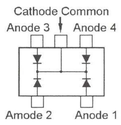
DTC144EK (26)
(Q3001)



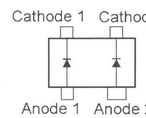
2SA1179 (M6)
(Q3002)



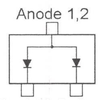
2SC2812 (L6)
(Q3011)



FMN1 (N1)
(D3002,3004,
3005,3006)



1SS319 (A4)
(D3003)



DAP202U (P)
(D3009)

Circuit Diagram

PANEL-UNIT F3601101

DS4001 FTD-15475AA

Q4005 LC75821E

Q4005 LC75821E

S4001 N5090095 POWER
S4002 N5090095 VFO/MR
S4003 N5090095 HOME
S4004 N5090095 SRCH
S4005 N5090095 SCAN
S4006 N5090095 LOW
S4007 N5090095 CNTL
S4008 N5090095 MUTE
S4009 N5090095 TONE
S4010 N5090095 RPT
S4011 N5090095 REV
S4012 N5090095 F/W

Normal: 0V
Press Any Key: 5V

D4001 DTA143EK
D4002 DTA143EK
D4003 VRPG4607K
D4004 DTA143EK
D4005 IMN10
D4006 VRPG4607K
D4007 IMN10
D4001 DA227

VHF RX: 4.71V
VHF TX: 0V
VHF RX: 0V
VHF TX: 4.96V
VHF RX: 0V
VHF TX: 4.71V
VHF RX: 4.96V
VHF TX: 0V

UHF RX: 4.71V
UHF TX: 0V
UHF RX: 0V
UHF TX: 4.96V
UHF RX: 0V
UHF TX: 4.71V
UHF RX: 4.96V
UHF TX: 0V

0V-7.2V

0.01V-5.04V
0.01V-5.04V

5.03V
4.15V

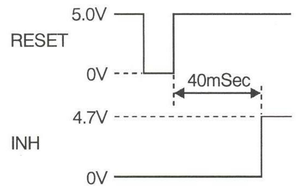
S4013 RH90N74AE20

To VR-R Unit J601 (See Page 4D-1)

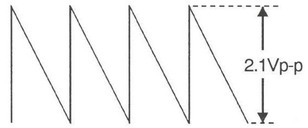
To VR-L Unit J501 (See Page 4C-1)

To CNTL Unit J3001 (See Page 4G-1)

① Q4005 Pin 57

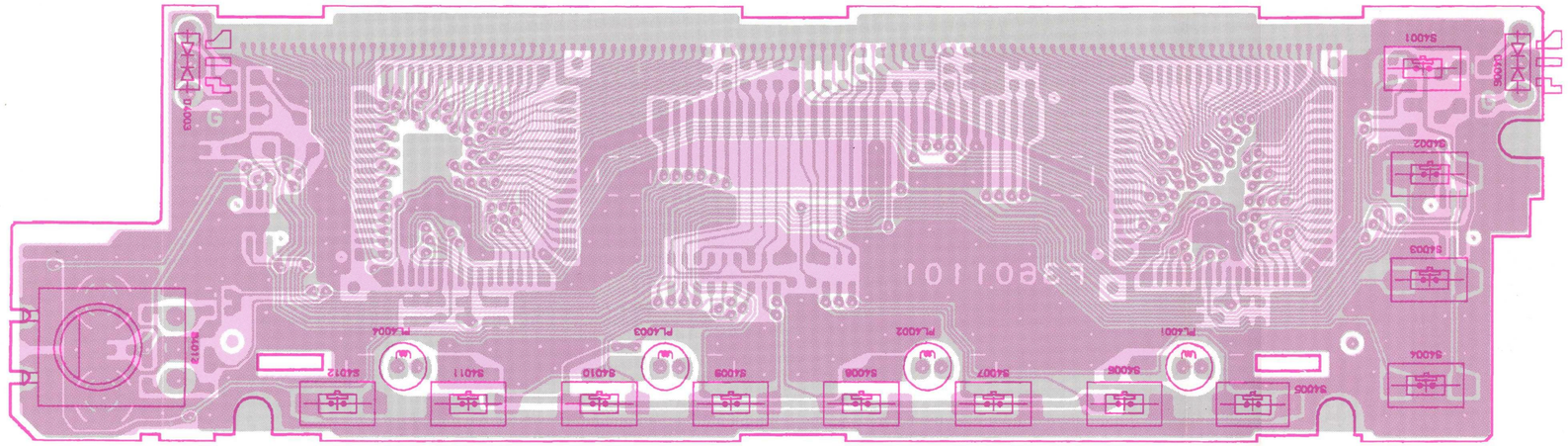


② Q4005 Pin 55 (50kHz)

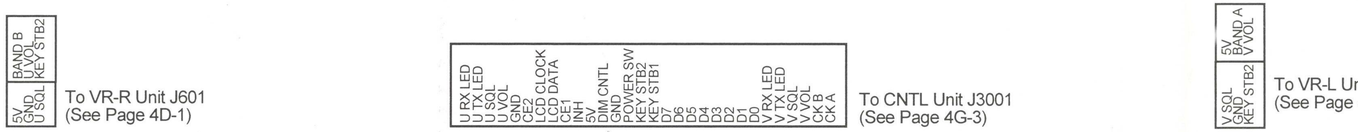


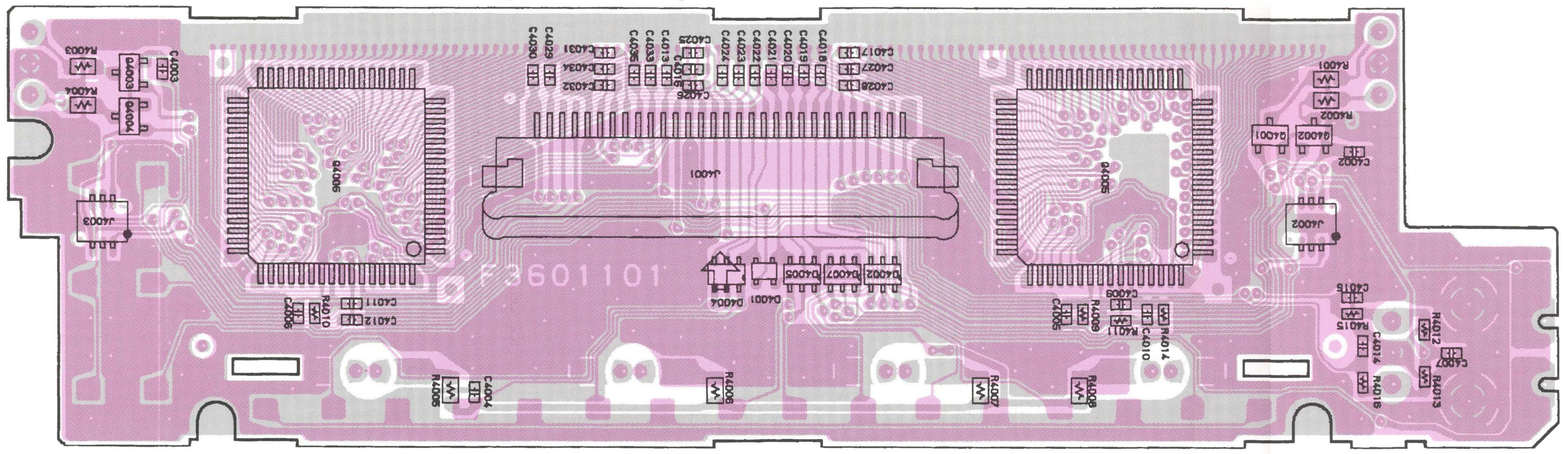
NOTE:
RESISTOR VALUES ARE IN Ω.1/16W :
CAPACITOR VALUES ARE IN μF. 50V :
UNLESS OTHERWISE NOTED.

Parts Layout

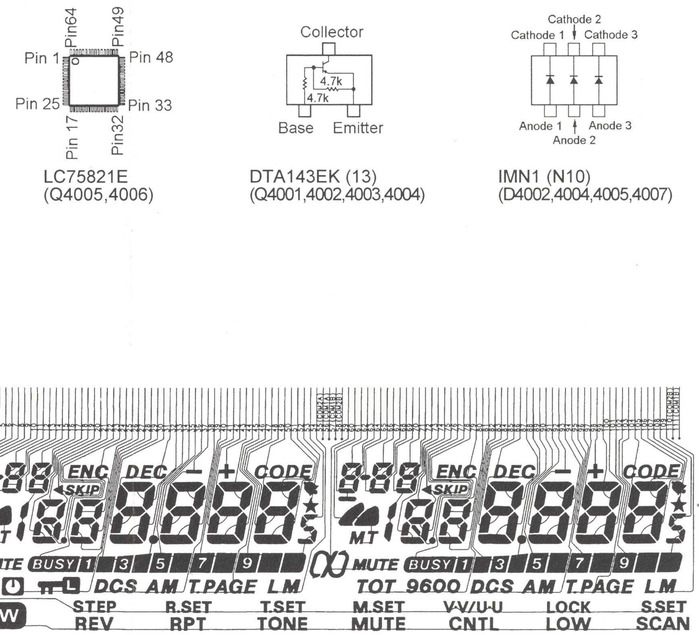


obverse view of LCD Side

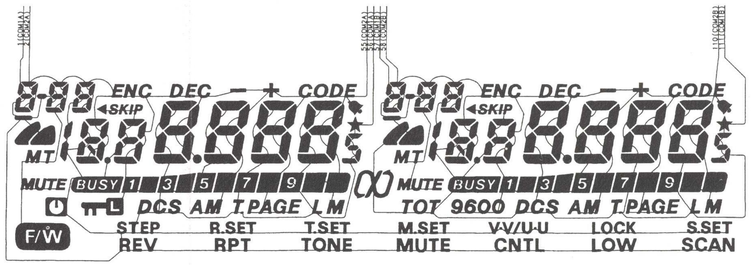




obverse view of component side



LCD Segmentation Circuit Diagram



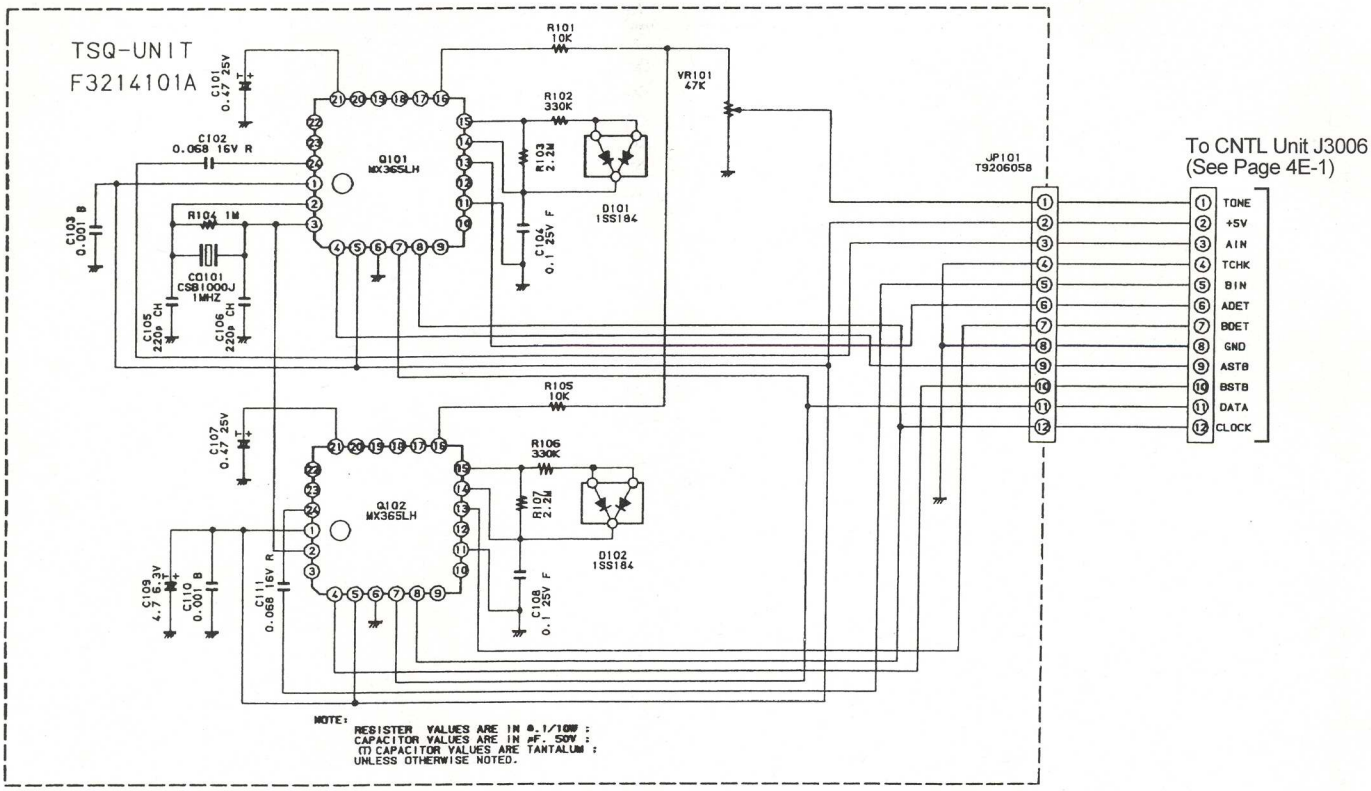
LCD Backplane Circuit Diagram

LC75821E
(Q4005,4006)

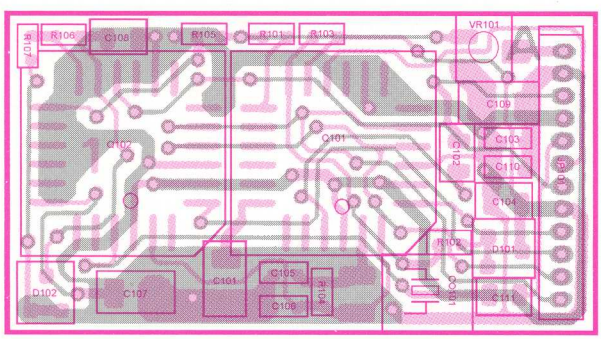
DTA143EK (13)
(Q4001,4002,4003,4004)

IMN1 (N10)
(D4002,4004,4005,4007)

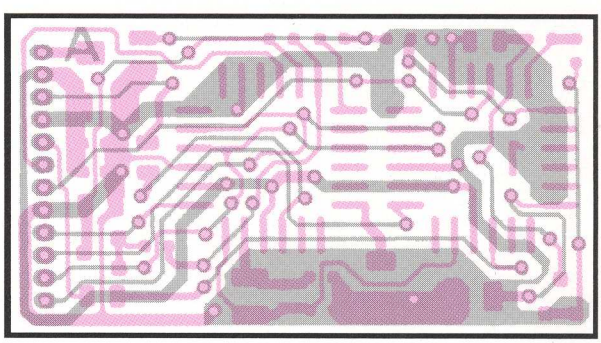
Circuit Diagram



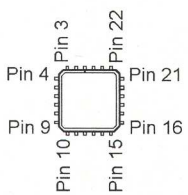
Parts Layout



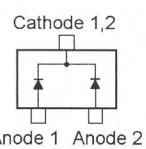
obverse view of connector side



obverse view of solder side

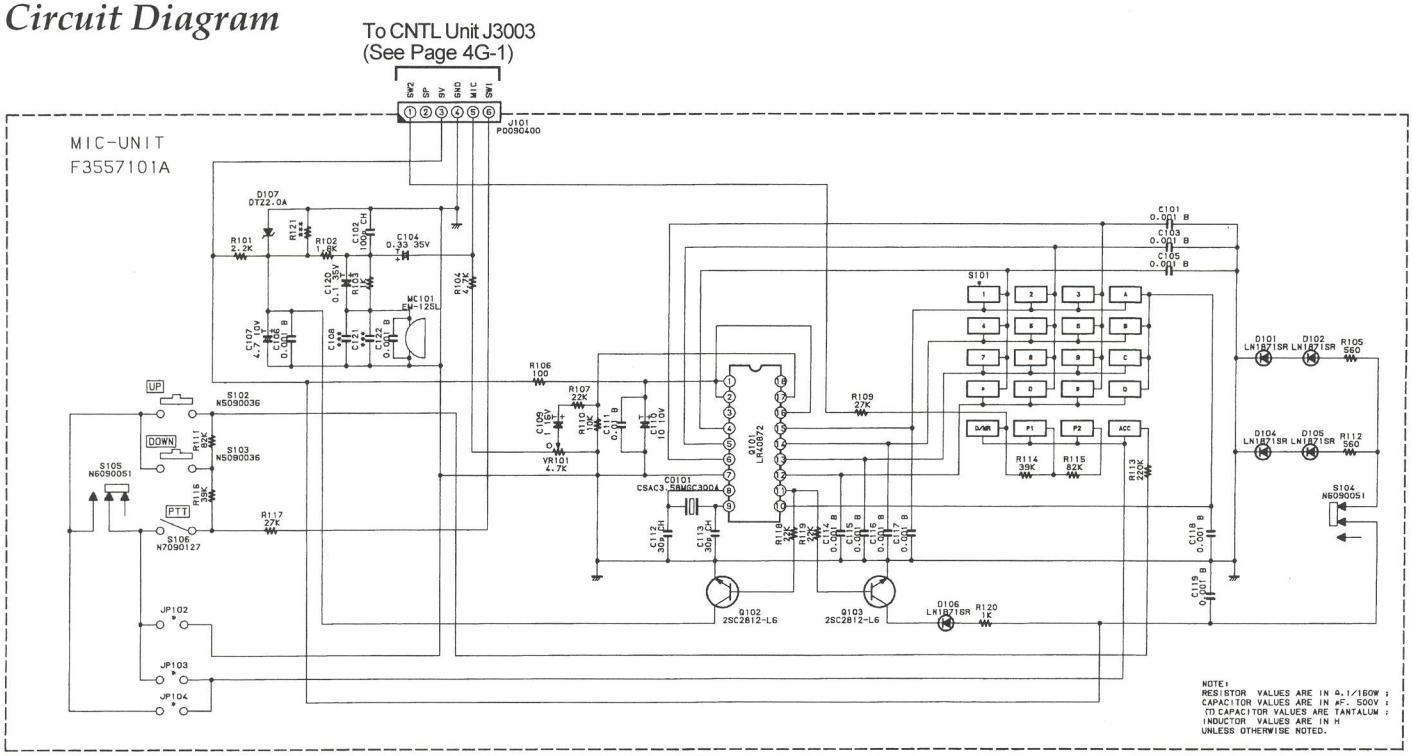


MX365LH
(Q101)

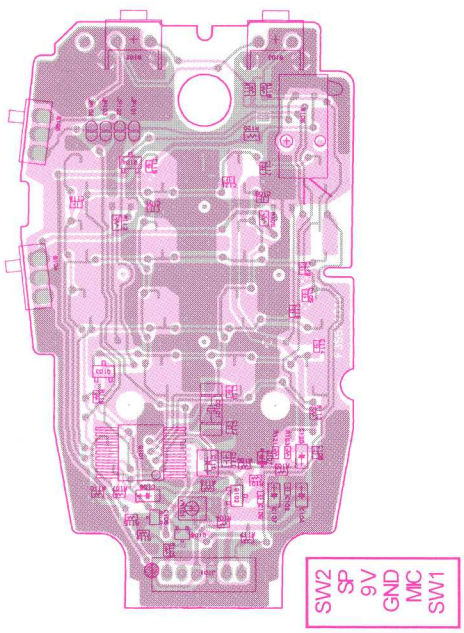


1SS301 (C3)
(D101)

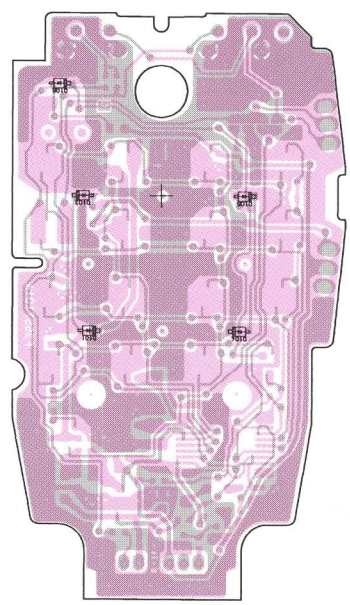
Circuit Diagram



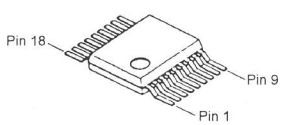
Parts Layout



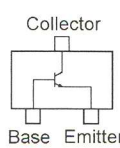
Connector Side



Solder Side



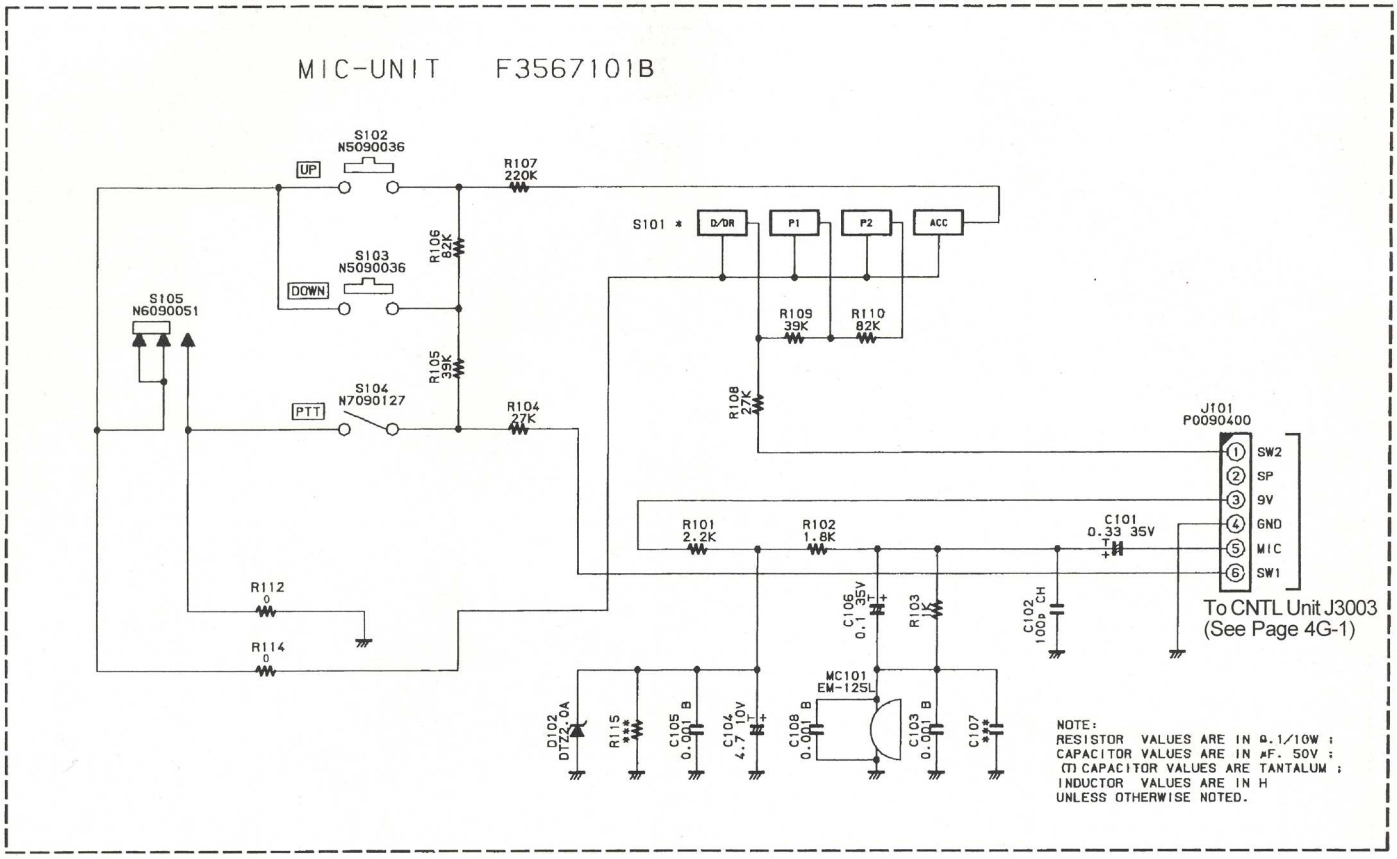
LR40872
(Q101)



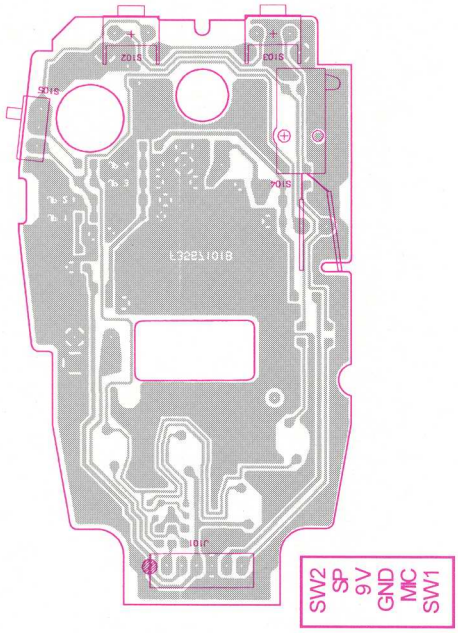
2SC2812 (L6)
(Q102,103)

MH-42B6J Hand Scanning Microphone

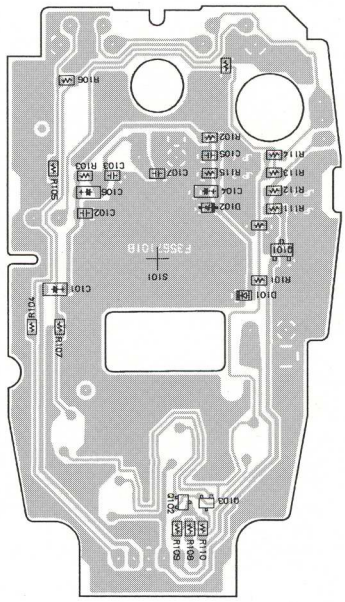
Circuit Diagram



Parts Layout



Connector Side



Solder Side