RDA5802E

SINGLE-CHIP BROADCAST FM RADIO TUNER

Rev.1.7–Jun.2009

1 General Description

The RDA5802E (RDA5802 Enhanced) is a single-chip broadcast FM stereo radio tuner with fully integrated synthesizer, IF selectivity and MPX decoder. The tuner uses the CMOS process, support multi-interface and require the least external component. The package size is 4X4mm and is completely adjustment-free. All these make it very suitable for portable devices.

The RDA5802E has a powerful low-IF digital audio processor, this make it have optimum sound quality with varying reception conditions.

The RDA5802E can be tuned to the worldwide frequency band.

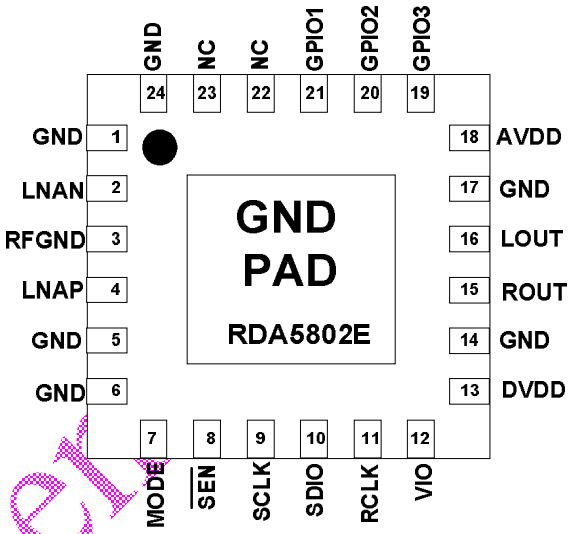


Figure 1-1. RDA5802E Top View

1.1 Features

- CMOS single-chip fully-integrated FM tuner
- Low power consumption
  - Total current consumption lower than 22mA at 3.0V power supply
- Support worldwide frequency band
  - 65 -108 MHz
- Digital low-IF tuner
  - Image-reject down-converter
  - High performance A/D converter
  - IF selectivity performed internally
- Fully integrated digital frequency synthesizer
  - Fully integrated on-chip RF and IF VCO
  - Fully integrated on-chip loop filter
- Autonomous search tuning
- Support 32.768KHz crystal oscillator
- Digital auto gain control (AGC)
- Digital adaptive noise cancellation
  - Mono/stereo switch
  - Soft mute
  - High cut
- Programmable de-emphasis (50/75 μs)
- Receive signal strength indicator (RSSI)
- Bass boost
- Volume control
- I^2S digital output interface
- Line-level analog output voltage
- 32.768 KHz 12M,24M,13M,26M,19.2M,38.4MHz Reference clock
- 2-wire and 3-wire serial control bus interface
- Directly support 32Ω resistance loading
- Integrated LDO regulator
  - 1.8 to 5.5 V operation voltage
- 4X4mm 24 pin QFN package

1.2 Applications

- Cellular handsets
- MP3, MP4 players
- Portable radios，PDAs, Notebook

2 Table of Contents

3 Functional Description

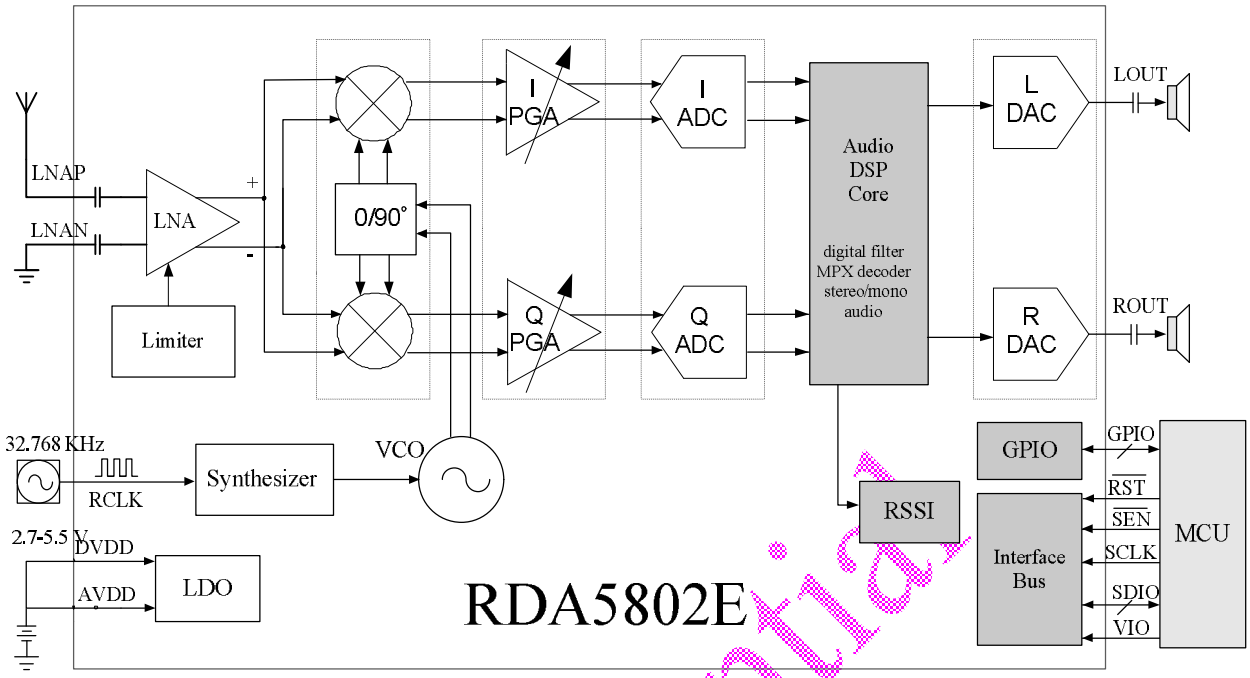


Figure 3-1. RDA5802E FM Tuner Block Diagram

3.1 FM Receiver

The receiver uses a digital low-IF architecture that avoids the difficulties associated with direct conversion while delivering lower solution cost and reduces complexity, and integrates a low noise amplifier (LNA) supporting the FM broadcast band (65 to 108MHz), a quadrature image-reject mixer, a programmable gain control (PGA), a high resolution analog-to-digital converters (ADCs), an audio DSP and a high-fidelity digital-to-analog converters (DACs).

The LNA has differential input ports (LNAP and LNAN) and supports any input port by set according registers bits (LNA_PORT_SEL[1:0]). It default input common mode voltage is GND.

The limiter prevents overloading and limits the amount of intermodulation products created by strong adjacent channels.

The quadrature mixer down converts the LNA output differential RF signal to low-IF, it also has image-reject function.

The PGA amplifies the mixer output IF signal and then digitized with ADCs.

The DSP core finishes the channel selection, FM demodulation, stereo MPX decoder and output audio signal. The MPX decoder can autonomous switch from stereo to mono to limit the output noise.

The DACs convert digital audio signal to analog and change the volume at same time. The DACs has low-pass feature and -3dB frequency is about 30 KHz.

3.2 Synthesizer

The frequency synthesizer generates the local oscillator signal which divide to quadrature, then be used to downconvert the RF input to a constant low intermediate frequency (IF). The synthesizer reference clock is 32.768 KHz.

The synthesizer frequency is defined by bits CHAN[9:0] with the range from 65MHz to 108MHz.

3.3 Power Supply

The RDA5802E integrated one LDO which supplies power to the chip. The external supply

voltage range is 1.8-5.5 V.

3.4 RESET and Control Interface select

The RDA5802E is RESET itself When VIO is Power up. And also support soft reset by trigger 02H BIT1 from 0 to 1. The control interface is select by MODE Pin. The MODE Pin is low ,I2C Interface is select. The MODE Pin is set to VIO, SPI Interface is select.

3.5 Control Interface

The RDA5802E supports three- wire and I^2C control interface. User could select either of them to program the chip.

The three-wire interface is a standard SPI interface. It includes three pins: $\overline{SEN}$, SCLK and SDIO. Each register write is 25-bit long, including 4-bit high register address, a r/w bit, 4-bit low register address, and 16-bit data (MSB is the first bit). RDA5802E samples command byte and data at posedge of SCLK. Each register read is also 25-bit long, including 4-bit high register address, a r/w bit, 4-bit low register address, and 16-bit data (MSB is the first bit) from RDA5802E. The turn around cycle between command byte from MCU and data from RDA5802E is a half cycle. RDA5802E samples command byte at posedge of SCLK, and output data also at posedge of SCLK.

The I^2C interface is compliant to I^2C Bus Specification 2.1. It includes two pins: SCLK and SDIO. A I^2C interface transfer begins with START condition, a command byte and data bytes, each byte has a followed ACK (or NACK) bit, and ends with STOP condition. The command byte includes a 7-bit chip address (0010000b) and a R/W bit. The ACK (or NACK) is always sent out by receiver. When in write transfer, data bytes is written out from MCU, and when in read transfer, data bytes is read out from RDA5802E. There is no visible register address in I^2C interface transfers. The I^2C interface has a fixed start register address (0x02h for write transfer and 0x0Ah for read transfer), and an internal incremental address counter. If register address meets the end of register file, 0x3Ah, register address will wrap back to 0x00h. For write transfer, MCU programs registers from register 0x02h high byte, then register 0x02h low byte, then register 0x03h high byte, till the last register. RDA5802E always gives out ACK after every byte, and MCU gives out STOP condition when register programming is finished. For read transfer, after command byte from MCU, RDA5802E sends out register 0x0Ah high byte, then register 0x0Ah low byte, then register 0x0Bh high byte, till receives NACK from MCU. MCU gives out ACK for data bytes besides last data byte. MCU gives out NACK for last data byte, and then RDA5802E will return the bus to MCU, and MCU will give out STOP condition.

Details refer to *RDA5802E Programming Guide*.

3.6 I^2S Audio Data Interface

The RDA5802E supports I^2S (Inter_IC Sound Bus) audio interface. The interface is fully compliant with I^2S bus specification. When setting I2SEN bit high, RDA5802E will output SCK, WS, SD signals from GPIO3, GPIO1, GPIO2 as I^2S master and transmitter, the sample rate is 48Kbps , 44.1kbps,32kbps….. RDA5802E also support as I^2S slaver mode and transmitter, the sample rate is less than 100kbps.

Details refer to *RDA5802E Programming Guide*.

3.7 GPIO Outputs

The RDA5802E has three GPIOs. The function of GPIOs could programmed with bits GPIO1[1:0], GPIO2[1:0], GPIO3[1:0] and I2SEN.

If I2SEN is set to low, GPIO pins could be programmed to output low or high or high-Z, or be programmed to output interrupt and stereo indicator with bits GPIO1[1:0], GPIO2[1:0], GPIO3[1:0]. GPIO2 could be programmed to output a low interrupt (interrupt will be generated only with interrupt enable bit STCIEN is set to high) when seek/tune process completes. GPIO3 could be programmed to output stereo indicator bit ST.

Constant low, high or high-Z functionality is available regardless of the state of VA and VD supplies or the ENABLE bit.

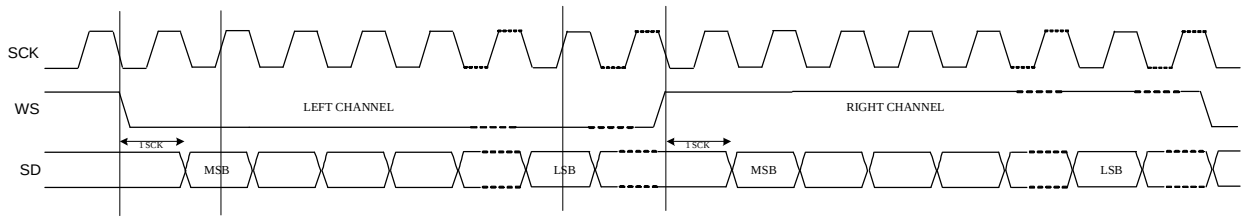


Figure 3-2. I2S Digital Audio Format

4 Electrical Characteristics

Table 4-1 DC Electrical Specification (Recommended Operation Conditions):

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
AVDD	Analog Supply Voltage	1.8	3.3	5.5	V
DVDD	Digital Supply Voltage	1.8	3.3	5.5	V
VIO	Interface Supply Voltage	1.5	-	3.6	V
T_{amb}	Ambient Temperature	-20	27	+70	℃
V_{IL}	CMOS Low Level Input Voltage	0		0.3*DVDD	V
V_{IH}	CMOS High Level Input Voltage	0.7*VDD		DVDD	V
V_{TH}	CMOS Threshold Voltage		0.5*VDD		V

Table 4-2 DC Electrical Specification (Absolute Maximum Ratings):

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
VIO	Interface Supply Voltage	-0.5		+4	V
T_{amb}	Ambient Temperature	-40		+90	°C
I_{IN}	Input Current(1)	-10		+10	mA
V_{IN}	Input Voltage(1)	-0.3		VIO+0.3	V
V_{lna}	LNA FM Input Level			-20	dBm

Notes:

1. For Pin: SCLK, SDIO, $\overline{SEN}$, MODE

Table 4-3 Power Consumption Specification

(VDD = 1.8 to 5.5 V, T_A = -25 to 85 ℃, unless otherwise specified)

SYMBOL	DESCRIPTION	CONDITION	TYP	UNIT
I_A	Analog Supply Current	ENABLE=1	18	mA
I_D	Digital Supply Current	ENABLE=1	3	mA
I_{VIO}	Interface Supply Current	SCLK and RCLK inactive	90	μA
I_{APD}	Analog Powerdown Current	ENABLE=0	2	μA
I_{DPD}	Digital Powerdown Current	ENABLE=0	2	μA
I_{VIO}	Interface Powerdown Current	ENABLE=0	10	μA

5 Receiver Characteristics

Table 5-1 Receiver Characteristics

(VDD = 2.7 to 5.5 V, T_A = -25 to 85 °C, unless otherwise specified)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
General specifications						
F_{in}	FM Input Frequency	BAND=00	87		108	MHz
		BAND=01	76		91	MHz
		BAND=10	76		108	MHz
		BAND=11	65		76	MHz
V_{rf}	Sensitivity[1,2,3]	(S+N)/N=26dB		1	1.5	μV EMF
R_{in}	LNA Input Resistance [7]			150		Ω
C_{in}	LNA Input Capacitance [7]		2	4	6	pF
$IP3_{in}$	Input IP3[4]	AGCD=1	80		-	dBμV
α_{am}	AM Suppression[1,2]	m=0.3	40		-	dB
S_{200}	Adjacent Channel Selectivity	±200KHz	45		-	dB
V_{AFL}; V_{AFR}	Left and Right Audio Frequency Output Voltage (Pins LOUT and ROUT)	Volume [3:0] =1111		200		mV
(S+N)/N	Maximum Signal Plus Noise to Noise Ratio[1,2,3,5]		55	60	-	dB
α_{SCS}	Stereo Channel Separation		35	-	-	dB
THD	Audio Total Harmonic Distortion[1,3,6]			0.03	0.05	%
α_{AOI}	Audio Output L/R Imbalance				0.1	dB
R_L	Audio Output Loading Resistance	Single-ended	32	-	-	Ω
Pins LNAN, LNAP, LOUT, ROUT and NC(22,23)						
V_{com_rfin}	Pins LNAN and LNAP Input Common Mode Voltage			**0**		V
V_{com}	Audio Output Common Mode Voltage[8]		0.95	1.	1.05	V
V_{com_nc}	Pins NC (22, 23) Common Mode Voltage			**Floating**		V
! The NC(22, 23) pins SHOULD BE left floating.						

Notes:

1. F_{in}=65 to 108MHz; F_{mod}=1KHz; de-emphasis=75μs; MONO=1; L=R unless noted otherwise;
2. Δf=22.5KHz;
3. B_{AF} = 300Hz to 15KHz, RBW <=10Hz;
4. $|f_2-f_1|$>1MHz, $f_0=2xf_1-f_2$, AGC disable, F_{in}=76 to 108MHz;
5. P_{RF}=60dB$_U$V;
6. Δf=75KHz.
7. Measured at V_{EMF} = 1 m V, f_{RF} = 65 to 108MHz
8. At LOUT and ROUT pins

6 Serial Interface

6.1 Three-wire Interface Timing

Table 6-1 Three-wire Interface Timing Characteristics

(VDD = 2.7 to 5.5 V, T_A = -25 to 85 °C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
SCLK Cycle Time	t_{CLK}		35			ns
SCLK Rise Time	t_R				50	ns
SCLK Fall Time	t_F				50	ns
SCLK High Time	t_{HI}		10			ns
SCLK Low Time	t_{LO}		10			ns
SDIO Input, $\overline{SEN}$ to SCLK↑ Setup	t_s		10	-	-	ns
SDIO Input, to SCLK↑ Hold	t_h		10	-	-	ns
SCLK↑ to SDIO Output Valid	t_{cdv}	Read	2	-	10	ns
$\overline{SEN}$↑ to SDIO Output High Z	t_{sdz}	Read	2	-	10	ns
Digital Input Pin Capacitance					5	pF

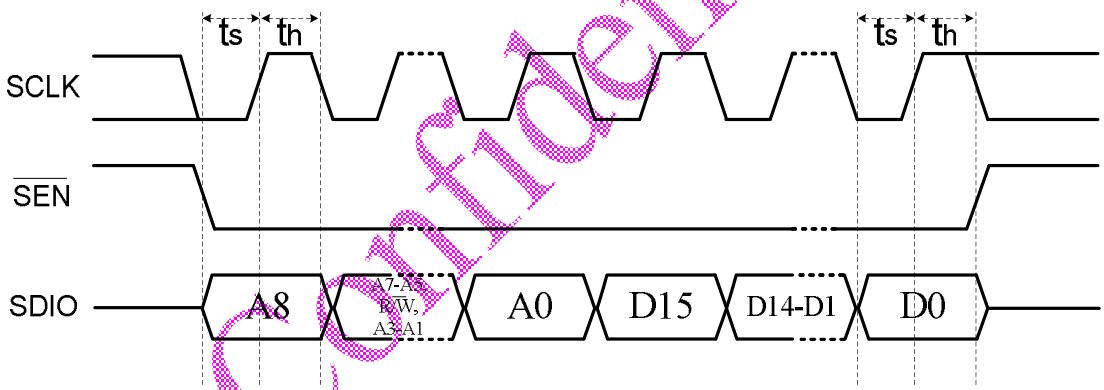


Figure 6-1. Three-wire Interface Write Timing Diagram

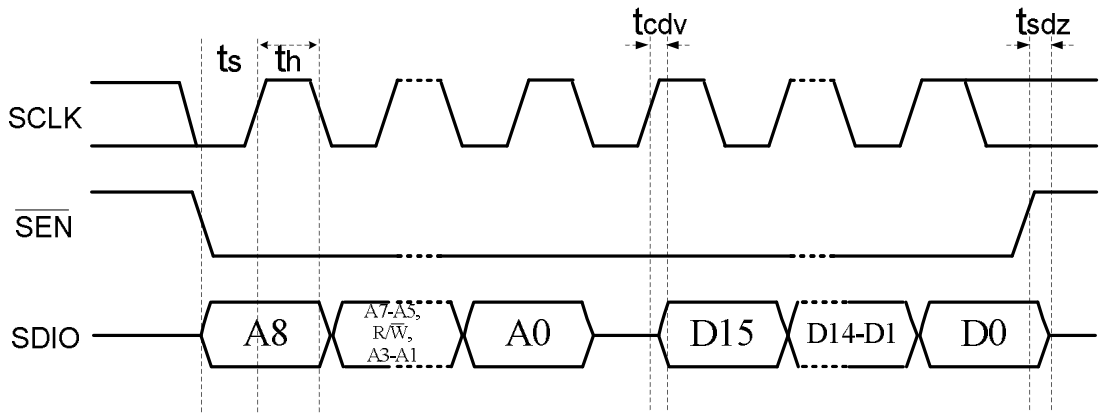


Figure 6-2. Three-wire Interface Read Timing Diagram

6.2 I²C Interface Timing

Table 6-2 I²C Interface Timing Characteristics

(VDD = 2.7 to 5.5 V, T_A = -25 to 85 °C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
SCLK Frequency	f_{scl}		0	-	400	KHz
SCLK High Time	t_{high}		0.6	-	-	µs
SCLK Low Time	t_{low}		1.3	-	-	µs
Setup Time for START Condition	$t_{su:sta}$		0.6	-	-	µs
Hold Time for START Condition	$t_{hd:sta}$		0.6	-	-	µs
Setup Time for STOP Condition	$t_{su:sto}$		0.6	-	-	µs
SDIO Input to SCLK↑ Setup	$t_{su:dat}$		100	-	-	ns
SDIO Input to SCLK↓ Hold	$t_{hd:dat}$		0	-	900	ns
STOP to START Time	t_{buf}		1.3	-	-	µs
SDIO Output Fall Time	$t_{f:out}$		$20+0.1C_b$	-	250	ns
SDIO Input, SCLK Rise/Fall Time	$t_{r:in}$ / $t_{f:in}$		$20+0.1C_b$	-	300	ns
Input Spike Suppression	t_{sp}		-	-	50	ns
SCLK, SDIO Capacitive Loading	C_b		-	-	50	pF
Digital Input Pin Capacitance					5	pF

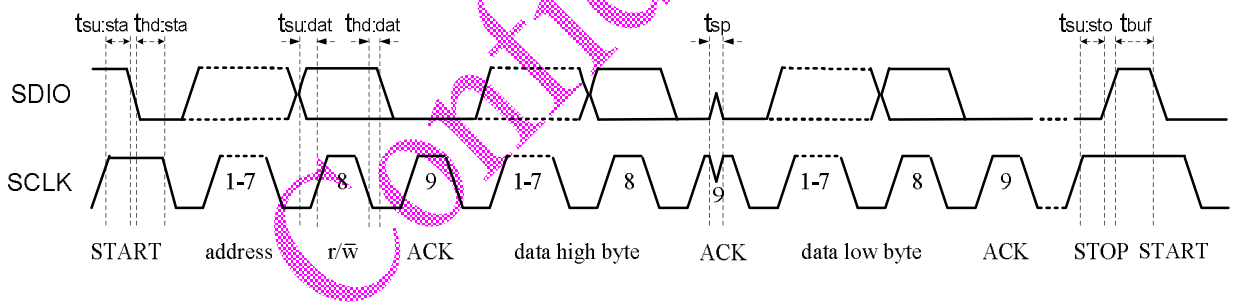


Figure 6-3. I²C Interface Write Timing Diagram

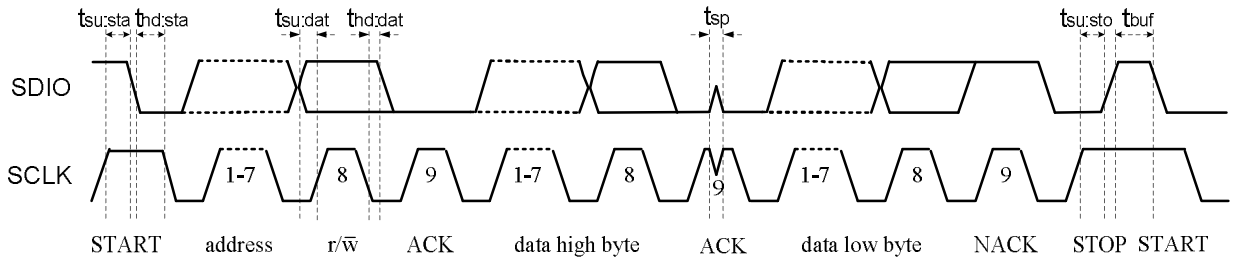


Figure 6-4. I²C Interface Read Timing Diagram

7 Register Definition

REG	BITS	NAME	FUNCTION	DEFAULT
00H	**15:8**	**CHIPID[7:0]**	**Chip ID.**	0x58
02H	**15**	**DHIZ**	**Audio Output High-Z Disable.** ***0 = High impedance; 1 = Normal operation***	0
	14	**DMUTE**	**Mute Disable.** ***0 = Mute; 1 = Normal operation***	0
	13	**MONO**	**Mono Select.** ***0 = Stereo; 1 = Force mono***	0
	12	**BASS**	**Bass Boost.** ***0 = Disabled; 1 = Bass boost enabled***	0
	10	**CLK_DIRECT_MODE**	**Reference clk (32.768K,12M,…) direct input mode.** **0=clk_buffer mode;** **1=clk directly input mode**	0
	9	**SEEKUP**	**Seek Up.** ***0 = Seek down; 1 = Seek up***	0
	8	**SEEK**	**Seek.** ***0 = Disable stop seek; 1 = Enable*** ***Seek begins in the direction specified by* SEEKUP *and ends when a channel is found with* RSSI *level above* SEEKTH[5:0]*, or the entire band has been searched.*** ***The* SEEK *bit is set low and the* STC *bit is set high when the seek operation completes.***	0
	7	**SKMODE**	**Seek Mode** **0 = wrap at the upper or lower band limit and continue seeking** **1 = stop seeking at the upper or lower band limit**	0
	6:4	**CLK_MODE[2:0]**	**000=32.768kHz** **001=12Mhz** **101=24Mhz** **010=13Mhz** **110=26Mhz** **011=19.2Mhz** **111=38.4Mhz**	000
	1	**SOFT_RESET**	**Soft reset.** **If 0, not reset;** **If 1, reset.**	0
	0	**ENABLE**	**Power Up Enable.** ***0 = Disabled; 1 = Enabled***	0
03H	**15:6**	**CHAN[9:0]**	**Channel Select.** **BAND =** ***0*** ***Frequency =*** ***Channel Spacing (kHz) x* CHAN+ *87.0 MHz*** **BAND =** ***1or 2*** ***Frequency =***	0x00

REG	BITS	NAME	FUNCTION	DEFAULT
			Channel Spacing (kHz) x* CHAN + *76.0 MHz **BAND = *3*** ***Frequency* =** ***Channel Spacing (kHz) x* CHAN + *65.0 MHz*** **CHAN *is updated after a seek operation.***	
	4	**TUNE**	**Tune** **0 = Disable** **1 = Enable** **The tune operation begins when the TUNE bit is set high. The STC bit is set high when the tune operation completes.** **The tune bit is reset to low automatically when the tune operation completes..**	0
	3:2	**BAND[1:0]**	**Band Select.** **00 = 87–108 MHz (US/Europe)** **01 = 76–91 MHz (Japan)** **10 = 76–108 MHz (world wide)** **11 = 65 –76 MHz （East Europe）**	00
	1:0	**SPACE[1:0]**	**Channel Spacing.** **00 = 100 kHz** **01 = 200 kHz** **10 = 50kHz**	00
04H	**14**	**STCIEN**	**Seek/Tune Complete Interrupt Enable.** **0 = Disable Interrupt** **1 = Enable Interrupt** **Setting STCIEN = 1 will generate a low pulse on GPIO2 when the interrupt occurs.**	0
	11	**DE**	**De-emphasis.** ***0 = 75 μs; 1 = 50 μs***	0
	9	**SOFTMUTE_EN**	**If 1, softmute enable**	1
	8	**AFCD**	**AFC disable.** **If 0, afc work;** **If 1, afc disabled.**	0
	6	**I2S_ENABLED**	**I2S bus enable** **If 0, disabled;** **If 1, enabled.**	0
	5:4	**GPIO3[1:0]**	**General Purpose I/O 3.** ***00 = High impedance*** ***01 = Mono/Stereo indicator (ST)*** ***10 = Low*** ***11 = High***	00
	3:2	**GPIO2[1:0]**	**General Purpose I/O 2.** ***00 = High impedance*** ***01 = Interrupt (INT)*** ***10 = Low*** ***11 = High***	00
	1:0	**GPIO1[1:0]**	**General Purpose I/O 1.**	00

REG	BITS	NAME	FUNCTION	DEFAULT
			00 = High impedance ***01 = Reserved*** ***10 = Low*** ***11 = High***	
05H	**15**	**INT _MODE**	**If 0, generate 5ms interrupt;** **If 1, interrupt last until read reg0CH action occurs.**	1
	14:8	**SEEKTH[6:0]**	**Seek Threshold. RSSI scale is logarithmic.** **0000000 = min RSSI**	0001000
	7:6	**LNA_PORT_SEL[1:0]**	**LNA input port selection bit:** **00: no input** **01: LNAN** **10: LNAP** **11: dual port input**	10
	5:4	**LNA_ICSEL_BIT[1:0]**	**Lna working current bit:** **00=1.8mA** **01=2.1mA** **10=2.5mA** **11=3.0mA**	10
	3:0	**VOLUME[3:0]**	**DAC Gain Control Bits (Volume).** ***0000=min; 1111=max*** ***Volume scale is logarithmic***	1111
06H	**12**	**I2s_mode_select**	**If 0, master mode;** **If 1, slave mode.**	0
	7:4	**I2s_ws_cnt[4:0]** **Only valid** **in master mode**	**4'b1000: WS_STEP_48;** **4'b0111: WS_STEP=44.1kbps;** **4'b0110: WS_STEP=32kbps;** **4'b0101: WS_STEP=24kbps;** **4'b0100: WS_STEP=22.05kbps;** **4'b0011: WS_STEP=16kbps;** **4'b0010: WS_STEP=12kbps;** **4'b0001: WS_STEP=11.025kbps;** **4'b0000: WS_STEP=8kbps;**	0000
0AH	**14**	**STC**	**Seek/Tune Complete.** **0 = Not complete** **1 = Complete** **The seek/tune complete flag is set when the seek or tune operation completes.**	0
	13	**SF**	**Seek Fail.** ***0 = Seek successful; 1 = Seek failure*** ***The seek fail flag is set when the seek operation fails to find a channel with an* RSSI *level greater than* SEEKTH[5:0].**	0
	10	**ST**	**Stereo Indicator.** ***0 = Mono; 1 = Stereo*** ***Stereo indication is available on* GPIO3 *by setting* GPIO1[1:0] =*01.***	1
	9:0	**READCHAN[9:0]**	**Read Channel.** **BAND = 0** **Frequency = Channel Spacing (kHz) x READCHAN[9:0]+ 87.0 MHz** **BAND = 1 or 2**	8'h00

REG	BITS	NAME	FUNCTION	DEFAULT
			Frequency = Channel Spacing (kHz) x READCHAN[9:0]+ 76.0 MHz **BAND = 3** **Frequency = Channel Spacing (kHz) x READCHAN[9:0]+ 65.0 MHz** **READCHAN[9:0] is updated after a tune or seek operation.**	
0BH	**15:9**	**RSSI[6:0]**	**RSSI.** **000000 = min** **111111 = max** **RSSI scale is logarithmic.**	0
	8	**FM TRUE**	**1 = the current channel is a station** **0 = the current channel is not a station**	0
	7	**FM_READY**	**1=ready** **0=not ready**	0

8 Pins Description

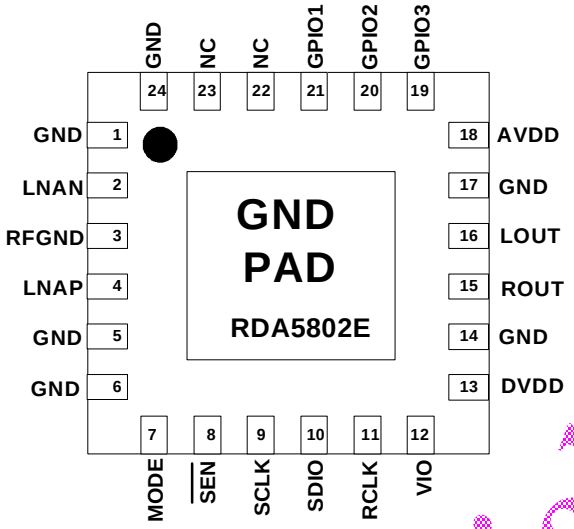
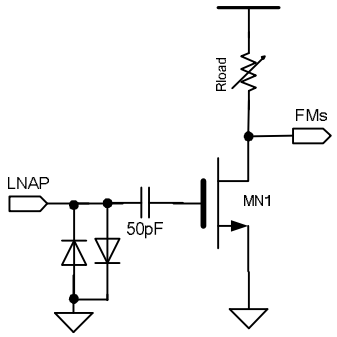
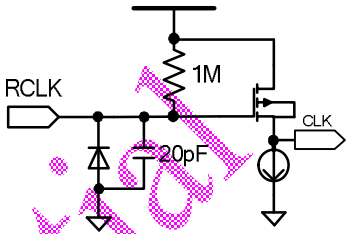
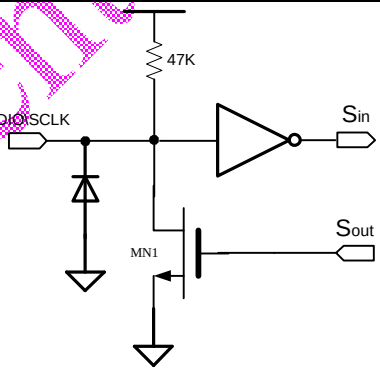
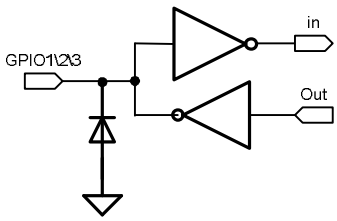


Figure 8-1. RDA5802E Top View

Table 8-1 RDA5802E Pins Description

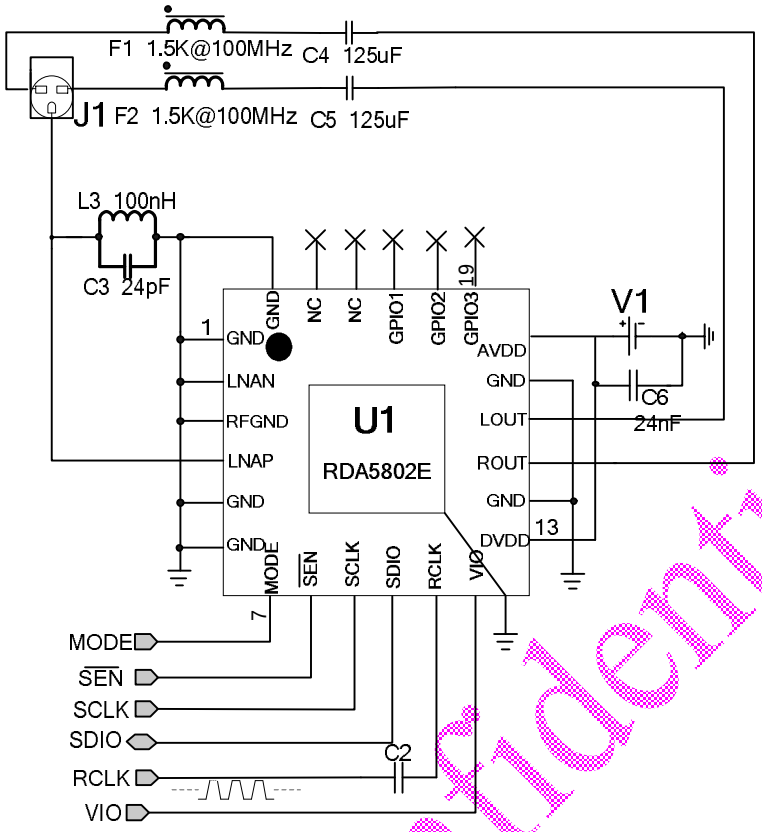
SYMBOL	PIN	DESCRIPTION
GND	1,5,6,14,17,24	Ground. Connect to ground plane on PCB
LNAN,LNAP	2,4	LNA input port. For single-ended input, LNAN should be connected to RFGND
RFGND	3	LNA ground. Connect to ground plane on PCB
MODE	7	Control Interface select The MODE Pin is low ,I2C Interface is select. The MODE Pin is set to VIO, SPI Interface is select.
$\overline{SEN}$	8	Latch enable (active low) input for serial control bus
SCLK	9	Clock input for serial control bus
SDIO	10	Data input/output for serial control bus
RCLK	11	32.768KHz crystal oscillator and reference clock input
VIO	12	Power supply for I/O
AVDD	18	Power supply for analog section
ROUT,LOUT	15,16	Right/Left audio output
DVDD	14	Power supply for digital section
GPIO1,GPIO2,GPIO3	19,20,21	General purpose input/output
NC	22,23	No Connect

Table 8-2 Internal Pin Configuration

SYMBOL	PIN	DESCRIPTION
LNAN/LNAP	2/4	
RCLK	11	
SCLK/SDIO	9/10	
GPIO1/GPIO2/GPIO3	19/20/21	

9 Application Diagram

9.1 Audio Loading Resistance Larger than 32Ω & TCXO Application:



Notes:

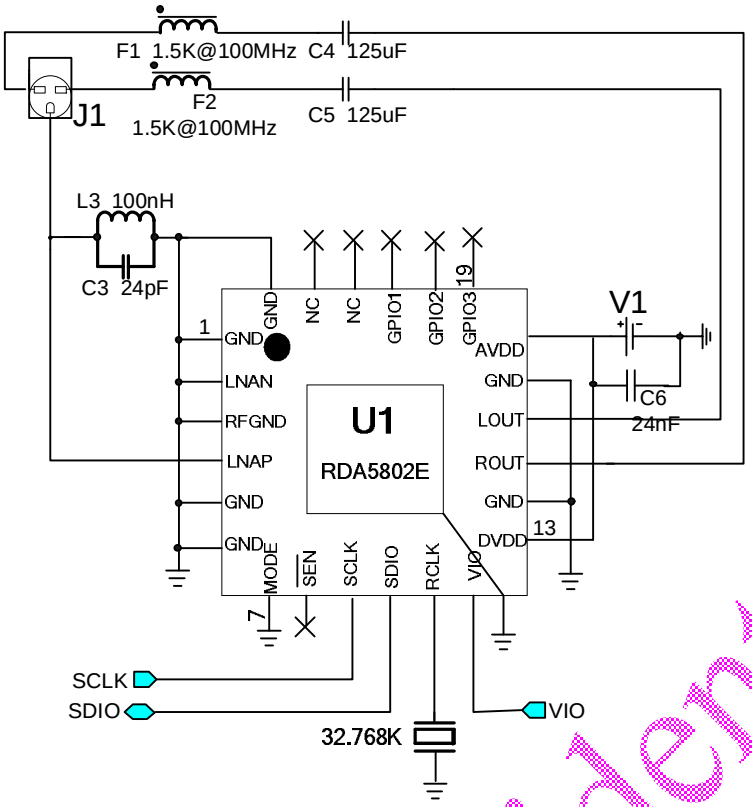
1. J1: Common 32Ω Resistance Headphone;
2. U1: RDA5802E Chip;
3. V1: Analog and Digital Power Supply (1.8~5.5V);
4. FM Choke (L3 and C3) for Audio Common and LNA Input Common;
5. Pins NC(22, 23), Should be Leaved Floating;
6. Set MODE to select control interface(GND—I2C,VIO—SPI);
6. Place C6 Close to AVDD pin.

Figure 9-1. RDA5802E FM Tuner Application Diagram (TCXO Application)

9.1.1 Bill of Materials:

COMPONENT	VALUE	DESCRIPTION	SUPPLIER
U1	RDA5802E	Broadcast FM Radio Tuner	RDA
J1		Common 32Ω Resistance Headphone	
C2	100pF	Couple CAP	Murata
L3/C3	100nH/24pF	LC Chock for LNA Input	Murata
C4,C5	125μF	Audio AC Couple Capacitors	Murata
C6	24nF	Power Supply Bypass Capacitor	Murata
F1/F2	1.5K@100MHz	FM Band Ferrite	Murata

9.2 Audio Loading Resistance Lower than 32Ω & DCXO Application:



Notes:

1. J1: Common 32Ω Resistance Headphone
2. U1: RDA5802E Chip
3. V1: Analog and Digital Power Supply (1.8~5.5V)
5. Pins NC(22, 23),Should be Leaved Floating;
6. Set MODE to select control interface(GND—I2C,VIO—SPI);
7. Place C6 Close to AVDD pin

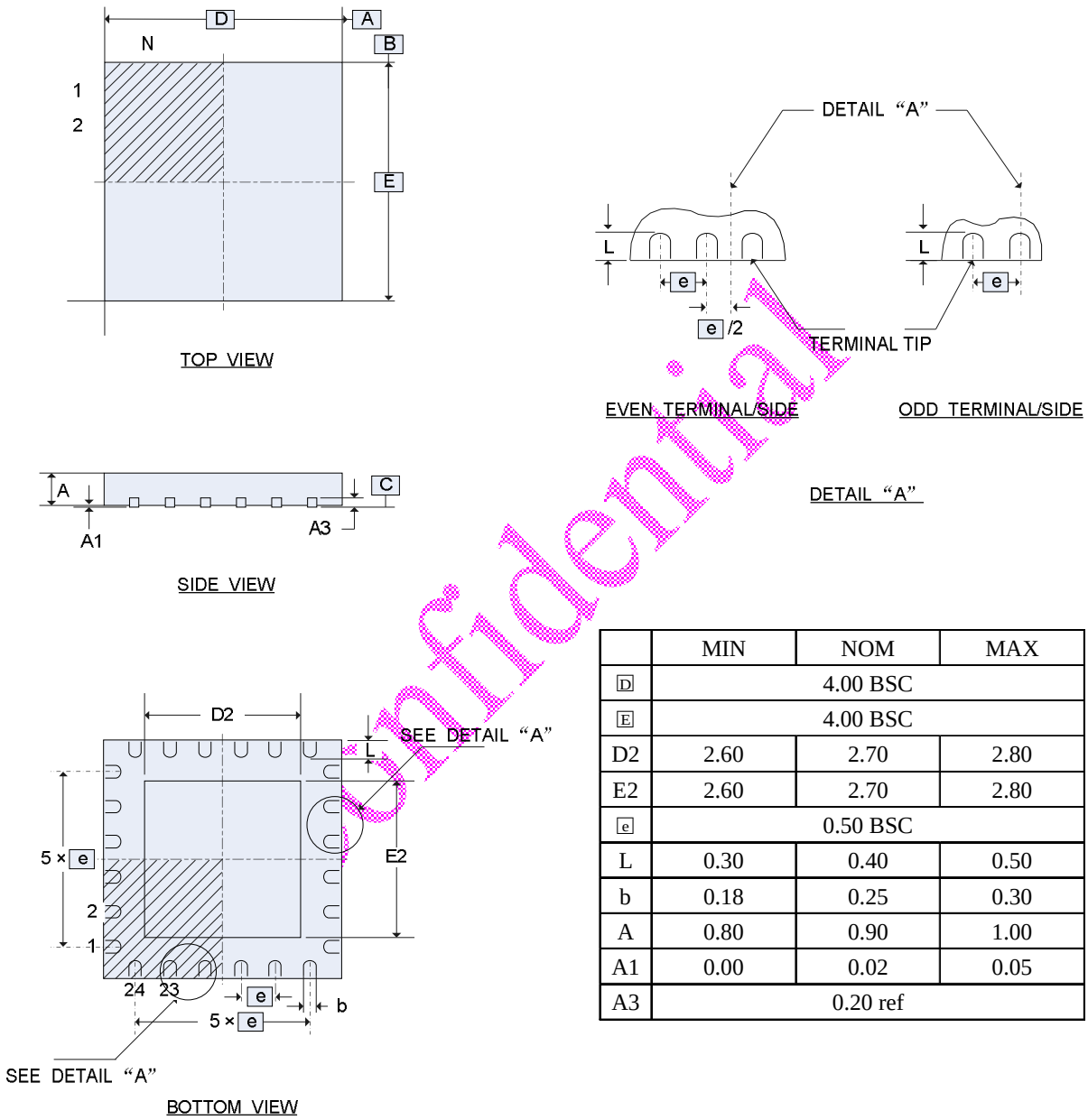
Figure 9-2. RDA5802E FM Tuner Application Diagram (32.768K crystal,I2C bus mode)

9.2.1 Bill of Materials:

COMPONENT	VALUE	DESCRIPTION	SUPPLIER
U1	RDA5802E	Broadcast FM Radio Tuner	RDA
J1		Audio Amplifier	
C4/C5	125uF	Audio AC Couple Capacitors	Murata
L3/C3	100nH/24pF	LC Chock for LNA Input	Murata
C6	24nF	Power Supply Bypass Capacitor	Murata
F1/F2	1.5K@100MHz	FM Band Ferrite	Murata

10 Package Physical Dimension

Figure 10-1 illustrates the package details for the RDA5802E. The package is lead-free and RoHS-compliant.



	MIN	NOM	MAX
D		4.00 BSC	
E		4.00 BSC	
D2	2.60	2.70	2.80
E2	2.60	2.70	2.80
e		0.50 BSC	
L	0.30	0.40	0.50
b	0.18	0.25	0.30
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A3		0.20 ref	

Figure 10-2. 24-Pin 4x4 Quad Flat No-Lead (QFN)

11 PCB Land Pattern

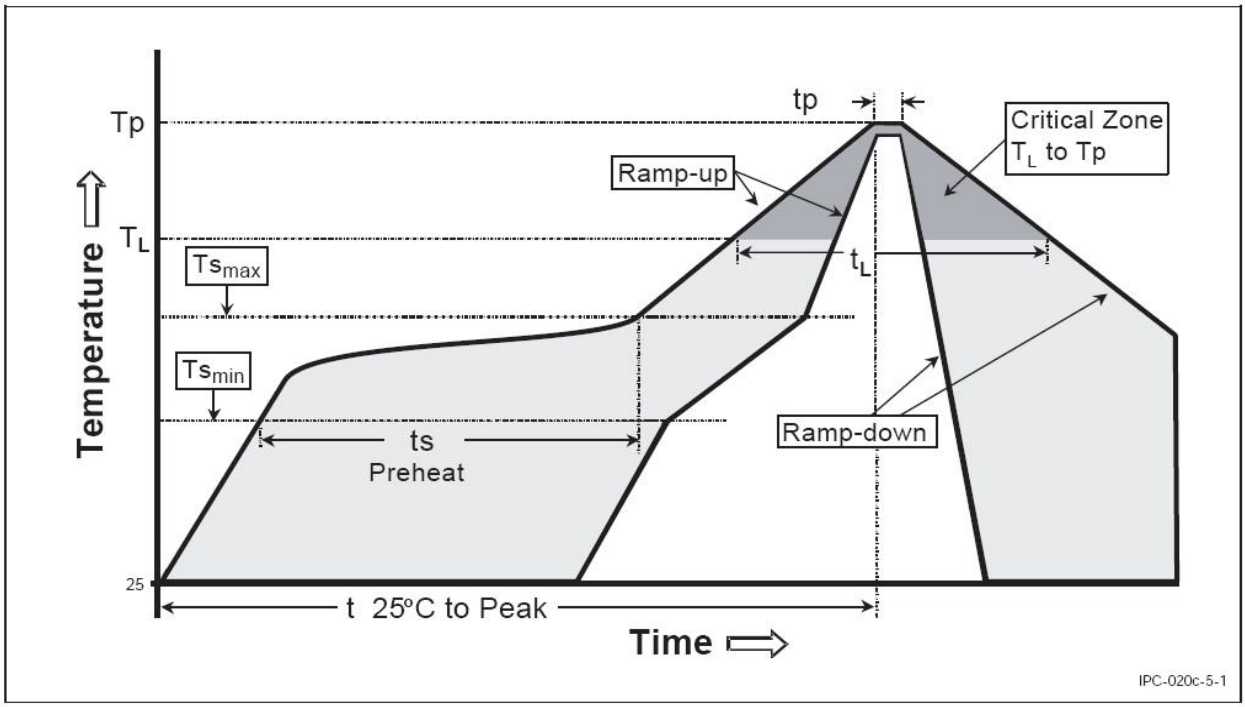


Figure 18.Classification Reflow Profile

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average Ramp-Up Rate (T_{Smax} to T_p)	3 °C/second max.	3 °C/second max.
Preheat -Temperature Min (T_{smin}) -Temperature Max (T_{smax}) -Time (t_{smin} to t_{smax})	 100 °C 100 °C 60-120 seconds	 150 °C 200 °C 60-180 seconds
Time maintained above: -Temperature (T_L) -Time (t_L)	 183 °C 60-150seconds	 217°C 60-150 seconds
Peak /Classification Temperature(T_p)	See Table-II	See Table-III
Time within 5 °C of actual Peak Temperature (t_p)	10-30 seconds	20-40 seconds
Ramp-Down Rate	6 °C/second max.	6 °C/seconds max.
Time 25 °C to Peak Temperature	6 minutes max.	8 minutes max.

Table-I Classification Reflow Profiles

Package Thickness	Volume mm^3 <350	Volume mm^3 ⩾350
＜2.5mm	240 + 0/-5 °C	225 + 0/-5 °C
⩾2.5mm	225 + 0/-5 °C	225 + 0/-5 °C

Table – II SnPb Eutectic Process – Package Peak Reflow Temperatures

Package Thickness	Volume mm^3 ＜350	Volume mm^3 350-2000	Volume mm^3 ＞2000
＜1.6mm	260 + 0 °C *	260 + 0 °C *	260 + 0 °C *
1.6mm – 2.5mm	260 + 0 °C *	250 + 0 °C *	245 + 0 °C *
⩾2.5mm	250 + 0 °C *	245 + 0 °C *	245 + 0 °C *
*Tolerance : The device manufacturer/supplier **shall** assure process compatibility up to and including the stated classification temperature(this mean Peak reflow temperature + 0 °C. For example 260+ 0 °C) at the rated MSL Level.			

Table – III Pb-free Process – Package Classification Reflow Temperatures

Note 1: All temperature refer topside of the package. Measured on the package body surface.

Note 2: The profiling tolerance is + 0 °C, - X °C (based on machine variation capability)whatever

is required to control the profile process but at no time will it exceed - 5 °C. The producer assures process compatibility at the peak reflow profile temperatures defined in Table –III.

Note 3: Package volume excludes external terminals(balls, bumps, lands, leads) and/or non integral heat sinks.

Note 4: The maximum component temperature reached during reflow depends on package the thickness and volume. The use of convection reflow processes reduces the thermal gradients between packages. However, thermal gradients due to differences in thermal mass of SMD package may sill exist.

Note 5: Components intended for use in a “lead-free” assembly process **shall** be evaluated using the “lead free” classification temperatures and profiles defined in Table-I II III whether or not lead free.

RoHS Compliant

The product does not contain lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls (PBB) or polybrominated diphenyl ethers (PBDE), and are therefore considered RoHS compliant.

ESD Sensitivity

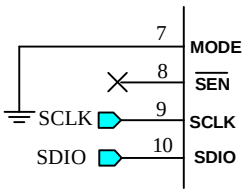
Integrated circuits are ESD sensitive and can be damaged by static electricity. Proper ESD techniques should be used when handling these devices.

12 Change List

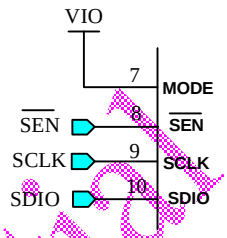
REV	DATE	AUTHER	CHANGE DESCRIPTION
V1.0	2009-03-03	ChunZhao	Original Draft.

13 Notes：

1: 通过硬件电路设置芯片工作总线控制模式，详细电路如下图：



附图：I2C 总线电路接口电路



SPI 总线电路接口电路

14 RDA5802E 与 RDA5802 对比

1、5802E 的 0x0Ch＝5803、0x0Dh＝5804，可以通过读这两个寄存器的缺省值来区别 5800、5802 和 5802E;
2、FM 天线尽量用第 4 脚（LNAP），不要用第 2 脚（LNAN）。5802E 的这两个输入脚电路结构是不一样的，性能有差别；
3、需要给客户说明 5802E 的 I2C 地址有三个：0010000；0010001；1100000（测试模式）
4、RCLK 脚接 32.768K 晶体的时候，要注意尽量减小寄生电容，PCB 走线不能太长；否则容易造成 32.768K 晶体不起振现象。
5、LNAN & LANP 管脚电路做了修改，直流电平必须为 0；如果客户天线的直流电平不为 0（比如瑞芯微的 MP3 芯片），则需要加 100pF 电容隔直。

	5802E	5802
ESD（静电）	5000V	2000V
I2C 缺省电平	不需要 sclk 触发	需要 sclk 下降沿触发
音量大小	大（250mV）	一般（200mV）
工作电压范围	1.8～5.5V (1.8~2V 性能略有下降)	2.7~5.5V
信噪比（SNR）	57dB	54dB
灵敏度（SEN）	-109dBm	-107dBm
工作电流	21.5mA	20mA
RDS	无	无
多参考时钟	可以任意设置参考时钟（需改寄存器）	普通
I2C 口抗毛刺	有提高	一般
硬件兼容性	普通情况下，全兼容 5802	
软件兼容性	普通情况下，全兼容 5802	
32K 时钟输入性	对 32K 时钟电平特性要求小。如果输入时钟信号幅度或者占空比小，可将 0x02h 寄存器 bit<10>设置成 1，这样参考时钟为直接输入模式，保证可靠性	如果 32K 时钟信号幅度过小或者占空比过小，会导致时钟信号输入困难

15 Contact Information

RDA Microelectronics (Shanghai), Inc.
Suite 1108 Block A, e-Wing Center, 113 Zhichun Road Haidian District, Beijing
Tel: 86-10-62635360
Fax: 86-10-82612663
Postal Code: 100086

Suite 302 Building 2, 690 Bibo Road Pudong District, Shanghai
Tel: 86-21-50271108
Fax: 86-21-50271099
Postal Code: 201203