



## Advance Information

# UHF Silicon FET Power Amplifier

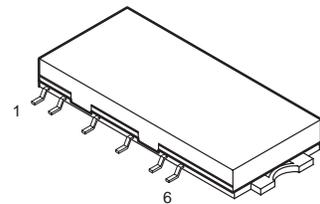
This device is designed specifically for TETRA digital 3.0 W mobile radios, operates from a 12.5 V supply and features 28 dB minimum gain.

- Specified 12.5 V Characteristics:
  - RF Input Power: 9.0 dBm
  - RF Output Power: 5.0 W
  - Power Gain: 28 dB Min
  - Harmonics:  $-30$  dBc Max @  $2 f_0$
- Metal Case Low Profile Gives Consistent Performance and Reliability
- $50 \Omega$  Input/Output Impedances
- Guaranteed Stability and Ruggedness

# MHW2723

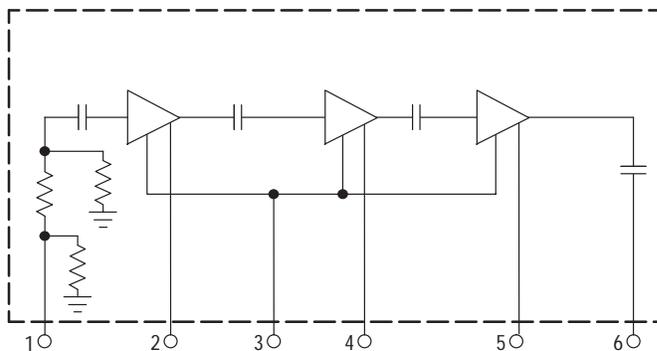
## UHF POWER AMPLIFIER 5.0 W, 380 to 470 MHz

### SEMICONDUCTOR TECHNICAL DATA



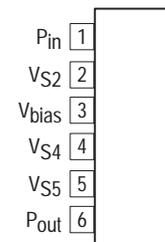
CASE 420Z

### Simplified Block Diagram



This device contains 3 active transistors.

### PIN CONNECTIONS



(Top View)

### ORDERING INFORMATION

Device	Operating Temperature Range	Package
MHW2723	$T_C = -30$ to $90^\circ\text{C}$	Power Module

# MHW2723

## MAXIMUM RATINGS (T<sub>C</sub> = 25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
DC Supply Voltage (Pins 2, 4, 5)	V <sub>S2, 4, 5</sub>	16	Vdc
DC Bias Voltage (Pin 3)	V <sub>bias</sub>	5.0	Vdc
RF Input Power	P <sub>in</sub>	14	dBm
RF Output Power (V <sub>S2, 4, 5</sub> = 16 V)	P <sub>out</sub>	12	W
Operating Case Temperature Range	T <sub>C</sub>	-30 to 90	°C
Storage Temperature Range	T <sub>stg</sub>	-30 to 100	°C

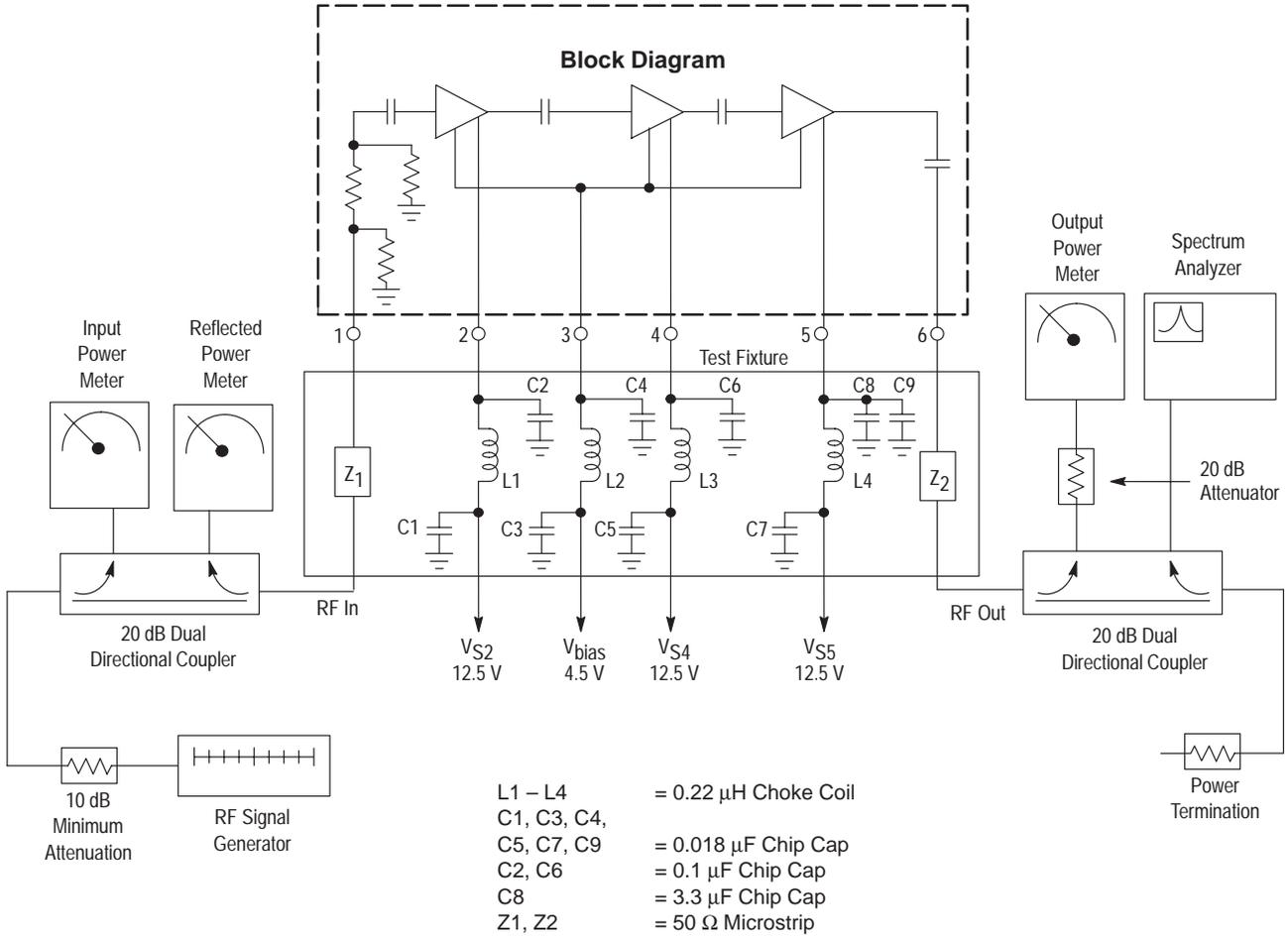
**NOTES:** 1. Meets Human Body Model (HBM) ≤3000 V.  
2. ESD data available upon request.

## ELECTRICAL CHARACTERISTICS (V<sub>bias</sub> = 4.5 V; V<sub>S2, 4, 5</sub> = 12.5 Vdc; T<sub>C</sub> = 25°C, 50 Ω system, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	BW	380	–	470	MHz
RF Input Power Range	P <sub>in</sub>	-8.0	–	14	dBm
Saturated Output Power (P <sub>in</sub> = 14 dBm) (Note 1)	P <sub>sat</sub>	12	–	–	W
Power Gain (Adjust P <sub>in</sub> for P <sub>out</sub> = 5.0 W)	G <sub>p</sub>	28	–	–	dB
Input Return Loss (P <sub>in</sub> = -8 to 14 dBm; 50 Ω Ref.)	VSWR <sub>in</sub>	–	–	2:1	–
Efficiency (P <sub>out</sub> = 5.0 W)	η	18	–	–	%
Adjacent Channel Power (P <sub>out</sub> = 5.0 W; f = f <sub>o</sub> ± 25 KHz, 18 KHz Bandwidth, π/4 DQPSK Modulation 36 KBITS/S, On/Off Factor 0.35) (Note 2)	ACP	-30	–	–	dBc
Alternate Channel Power (P <sub>out</sub> = 5.0 W; f = f <sub>o</sub> ± 50 KHz, 18 KHz Bandwidth, π/4 DQPSK Modulation 36 KBITS/S, On/Off Factor 0.35) (Note 2)	ACP	-40	–	–	dBc
Bias Current (V <sub>bias</sub> = 4.5 V)	I <sub>bias</sub>	–	–	10	mA
Rise Time (P <sub>out</sub> = 0.1 mW to 12 W) (Note 1)	t <sub>r</sub>	–	–	20	μsec
Stability (P <sub>out</sub> = -20 dBm Avg to 38 dBm Avg; V <sub>bias</sub> = 4.5 V Pulse Pin; V <sub>S2, 4, 5</sub> = 10.8–16 Vdc; Load VSWR = 2:1, Source VSWR = 2:1, All Phase Angles at Frequency of Test)	–	All Spurious Outputs More Than 60 dB Below Desired Signal			
Harmonics (P <sub>out</sub> = 5.0 W) 2 f <sub>o</sub>	–	–	–	-30	dBc
Isolation (V <sub>bias</sub> = 0 V; P <sub>in</sub> = Nominal Drive Level for P <sub>out</sub> = 12 W; V <sub>S2, 4, 5</sub> = 12.5 Vdc; Case Temperature = 25°C; Load Impedance and Source Impedance = 50 Ω)	–	–	–	60	dB
Load Mismatch Stress (V <sub>S2, 4, 5</sub> = 16 Vdc; V <sub>bias</sub> = 4.5 V; P <sub>in</sub> = 12 dBm; (25% Duty Cycle Period = 56.7 ms); Load VSWR = 2:1, All Phase Angles at Frequency of Test) (Note 1)	ψ	No Degradation in Output Power Before & After Test			
Noise Power (P <sub>out</sub> = 5.0 W; f = f <sub>o</sub> + 5.0 MHz; Bandwidth = 18 KHz)	P <sub>N</sub>	–	–	-85	dBm

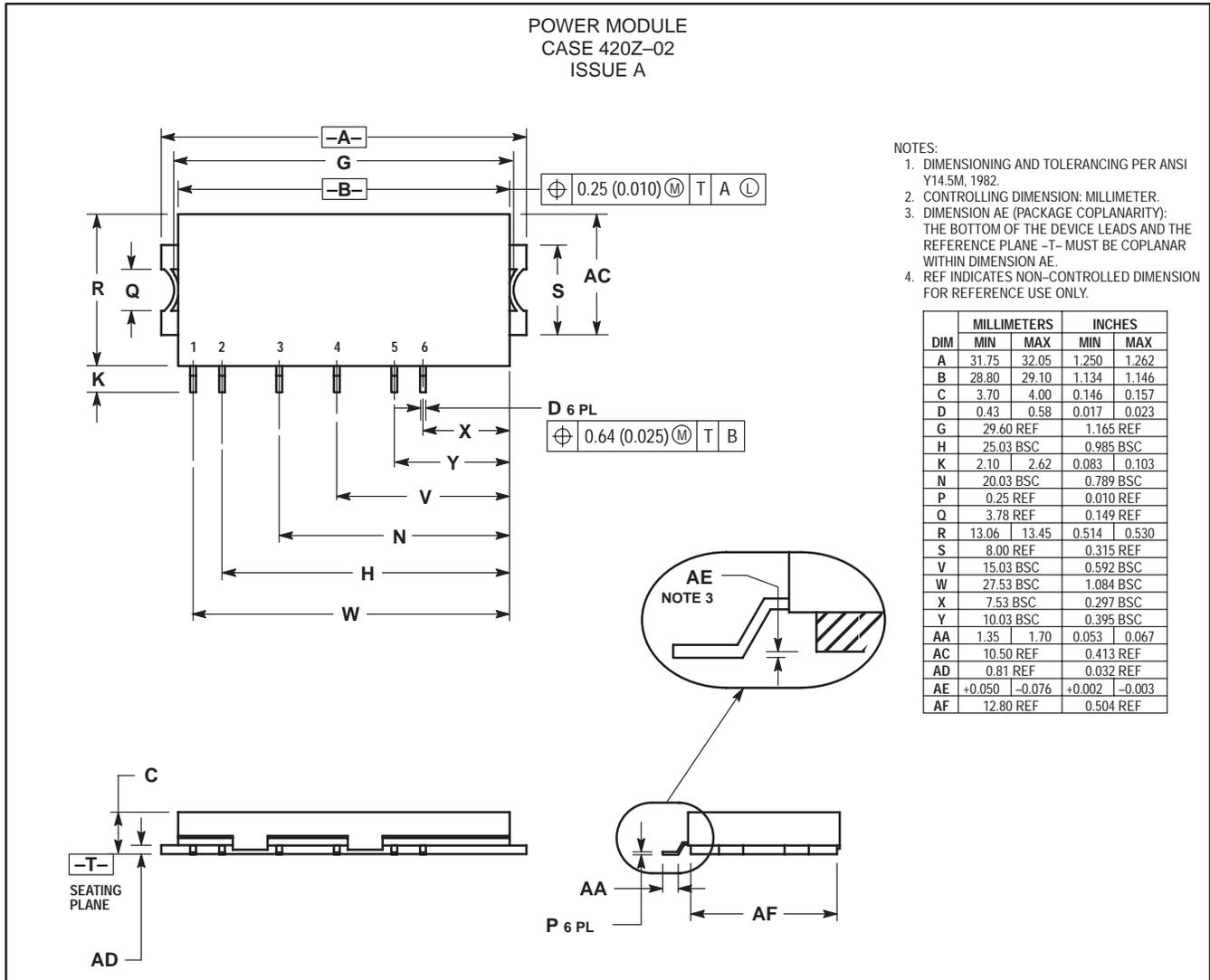
**NOTES:** 1. Pulsed V<sub>bias</sub> or P<sub>in</sub>; Duty Cycle = 25%, Period = 56.7 ms; On Time = 14.17 ms.  
2. TETRA Signal Format – Continuous Wave.

Figure 1. Test Circuit Diagram



# MHW2723

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