INTRODUCTION

This service manual describes the latest service information for the IC-R2 at the time of publication.

<table>
<thead>
<tr>
<th>MODEL</th>
<th>VERSION</th>
<th>SYMBOL</th>
</tr>
</thead>
<tbody>
<tr>
<td>IC-R2</td>
<td>Europe</td>
<td>EUR</td>
</tr>
<tr>
<td></td>
<td>Italy</td>
<td>ITA</td>
</tr>
<tr>
<td></td>
<td>Taiwan</td>
<td>TPE</td>
</tr>
<tr>
<td></td>
<td>U.S.A.</td>
<td>USA</td>
</tr>
<tr>
<td></td>
<td>Canada</td>
<td>CAN</td>
</tr>
<tr>
<td></td>
<td>Other</td>
<td>OTH</td>
</tr>
<tr>
<td></td>
<td></td>
<td>OTH-1</td>
</tr>
</tbody>
</table>

To upgrade quality, all electrical or mechanical parts and internal circuits are subject to change without notice or obligation.

DANGER

NEVER connect the receiver to an AC outlet or to a DC power supply that uses more than 3.5 V. Such a connection could cause a fire hazard and/or electric.

DO NOT expose the receiver to rain, snow or any liquids.

DO NOT reverse the polarities of the power supply when connecting the receiver.

DO NOT apply an RF signal of more than 20 dBm (100mW) to the antenna connector. This could damage the receiver's front end.

ORDERING PARTS

Be sure to include the following four points when ordering replacement parts:

1. 10-digit order numbers
2. Component part number and name
3. Equipment model name and unit name
4. Quantity required

<SAMPLE ORDER>

8930046581 LCD Contact IC-R2 LOGIC UNIT 5 pieces
8810009560 Screw PH BO M2x6 ZK IC-R2 Chassis 10 pieces

Addresses are provided on the inside back cover for your convenience.

REPAIR NOTES

1. Make sure a problem is internal before disassembling the receiver.
2. DO NOT open the receiver until the receiver is disconnected from its power source.
3. DO NOT force any of the variable components. Turn them slowly and smoothly.
4. DO NOT short any circuits or electronic parts. An insulated turning tool MUST be used for all adjustments.
5. DO NOT keep power ON for a long time when the receiver is defective.
6. READ the instructions of test equipment thoroughly before connecting equipment to the receiver.
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SECTION 1  SPECIFICATIONS

■ GENERAL

• Frequency range : 

<table>
<thead>
<tr>
<th>Version</th>
<th>Receive Frequencies (MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>EUR, U.K., CAN, OTH, OTH-1</td>
<td>0.495 – 1309.995</td>
</tr>
<tr>
<td>U.S.A.</td>
<td>0.495 – 823.995</td>
</tr>
</tbody>
</table>

| 849.000 – 868.995 |
| 894.000 – 1309.995 |

• Mode : FM, WFM, AM
• No. of memory channel : 450 channel
• Frequency stability : ±6 ppm max. (-10°C to +60°C)
• Tuning steps : 5, 6.25, 10, 12.5, 15, 20, 25, 30, 50, and 100 kHz
• Antenna Impedance : 50 Ω
• Power supply requirement : 2 × AA(R6) Ni-Cd or alkaline cell
• Polarity : Negative ground
• Frequency resolution : 5 kHz, 6.25 kHz
• Current drain (at 3.0 V) :
  - Rated audio : 170 mA typical
  - Standby : 100 mA typical
  - Power saved : 41 mA typical
• Usable temperature range : –10°C to +60°C (-14°F to +140°F)
• Dimensions : 58(W) × 86(H) × 27(D) mm; (projections not included) 2 9/32 (W) × 3 3/8 (H) × 1 1/16 (D) in
• Weight (with antenna and battery) : 170 (g); 6 (oz)
• External SP connector : 3-conductor 3.5(d) mm (1/8") / 8Ω

■ RECEIVER

• Receiver system : Tripple super heterodyne
• Intermediate frequency : 1st 266.7 MHz
  2nd 19.65 MHz
  3rd 450 kHz
• Sensitivity* : (except spurious points)

<table>
<thead>
<tr>
<th>Frequency (MHz)</th>
<th>FM</th>
<th>WFM</th>
<th>AM</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.495 – 1.625</td>
<td></td>
<td></td>
<td>2.5 µV</td>
</tr>
<tr>
<td>1.625 – 5.0</td>
<td>0.56 µV</td>
<td></td>
<td>1.8 µV</td>
</tr>
<tr>
<td>5.0 – 30.0</td>
<td></td>
<td></td>
<td>1.8 µV</td>
</tr>
<tr>
<td>30.0 – 76.0</td>
<td></td>
<td></td>
<td>1.8 µV</td>
</tr>
<tr>
<td>76.0 – 108.0</td>
<td>1.8 µV</td>
<td></td>
<td></td>
</tr>
<tr>
<td>108.0 – 118.0</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>118.0 – 136.0</td>
<td></td>
<td></td>
<td>1.8 µV</td>
</tr>
<tr>
<td>136.0 – 175.0</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>175.0 – 222.0</td>
<td></td>
<td></td>
<td>1.8 µV</td>
</tr>
<tr>
<td>222.0 – 247.0</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>247.0 – 330.0</td>
<td>0.56 µV</td>
<td></td>
<td>1.8 µV</td>
</tr>
<tr>
<td>330.0 – 470.0</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>470.0 – 770.0</td>
<td>2.5 µV</td>
<td></td>
<td></td>
</tr>
<tr>
<td>770.0 – 833.0</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>833.0 – 1309.995</td>
<td>0.79 µV</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

* FM and WFM are measured at 12 dB SINAD; AM is measured at 10 dB S/N.

• Squelch Sensitivity :

<table>
<thead>
<tr>
<th>Frequency (MHz)</th>
<th>FM</th>
<th>WFM</th>
<th>AM</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.495 – 1.625</td>
<td></td>
<td></td>
<td>2.5 µV</td>
</tr>
<tr>
<td>1.625 – 5.0</td>
<td>0.56 µV</td>
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<td>1.8 µV</td>
</tr>
<tr>
<td>5.0 – 30.0</td>
<td></td>
<td></td>
<td>1.8 µV</td>
</tr>
<tr>
<td>30.0 – 76.0</td>
<td></td>
<td></td>
<td>1.8 µV</td>
</tr>
<tr>
<td>76.0 – 108.0</td>
<td>1.8 µV</td>
<td></td>
<td></td>
</tr>
<tr>
<td>108.0 – 118.0</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>118.0 – 136.0</td>
<td></td>
<td></td>
<td>1.8 µV</td>
</tr>
<tr>
<td>136.0 – 175.0</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>175.0 – 222.0</td>
<td></td>
<td></td>
<td>1.8 µV</td>
</tr>
<tr>
<td>222.0 – 247.0</td>
<td></td>
<td></td>
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</tr>
<tr>
<td>247.0 – 330.0</td>
<td>0.56 µV</td>
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<td>1.8 µV</td>
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<tr>
<td>330.0 – 470.0</td>
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<td>0.79 µV</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

• Selectivity :
  - AM / FM : more than 15 kHz / –6 dB
  - WFM : less than 30 kHz / –60 dB
  - more than 150 kHz / –6 dB

• Audio output power : 100 mW typical at 10% distortion with an 8 Ω load

All stated specifications are subject to change without notice or obligation.
SECTION 2  INSIDE VIEWS

• LOGIC UNIT

- AF power amplifier (IC15: TA31056F)
- AF mute switch (Q37: 2SJ144)
- AF filter (Q30: XP6501)
- +3.2 regulator (IC4: S-81332H)
- 2nd mixer (IC10: µPC2757T)
- IF amplifier (Q5: 2SC5231)
- FM IF IC (IC2: TA31136FN)
- PLL circuit
- PLL reference oscillator (X1: CR593 19.200MHz)
- PLL IC (IC3: µPD3140GS)

• RF UNIT

TOP VIEW

- 2nd mixer (IC10: µPC2757T)
- IF amplifier (Q5: 2SC5231)
- FM IF IC (IC2: TA31136FN)
- PLL reference oscillator (X1: CR593 19.200MHz)
- PLL IC (IC3: µPD3140GS)

BOTTOM VIEW

- 1st mixer (IC1: µPC2757T)
- VCO circuit
SECTION 3 DISASSEMBLY INSTRUCTIONS

• REMOVING THE REAR PANEL
  1. Unscrew 2 screws, A.
  2. Remove the rear panel in the direction of the arrow.

• REMOVING THE RF UNIT
  1. Unscrew 1 screw, B.
  2. Remove 1 knob, C.
  3. Unscrew 2 nuts, D and E.
  4. Unsolder 5 points, F, and then remove the RF unit.

• REMOVING THE LOGIC UNIT
  1. Unscrew 2 screws, G.
  2. Unsolder 2 points, H, and then remove the LOGIC unit.
4-1 RECEPTOR CIRCUITS

4-1-1 ANTENNA SWITCHING CIRCUIT (RF UNIT)
The RF signals from the antenna connector pass through the limiter (D68) and an attenuator (D69). The signals are then applied to the RF circuit the antenna switching circuit (D13, D73, D75) which suppress out-of-band signals.

4-1-2 RF CIRCUIT (RF UNIT)
The RF circuit amplifies the received signals within the range of frequency coverage and filters out-of-band signals.

(1) 0.495 MHz–29.999 MHz
RF signals (0.495–29.999 MHz) from an antenna switching circuit (D73) pass through a low-pass filter (C511–C515, L81, L82). The filtered signals are amplified at an RF amplifier (Q505) passing through each band-pass filter depending on the receiving frequency. The amplified signals are then applied to the 1st mixer circuit (IC1) after being amplified at another RF amplifier (IC11) via the band switching diode (D71).

The signals below 1.9 MHz pass through a low-pass filter (C534, C535, C657, C658, L88, L89) via the band switching diode (D66), and are then applied to the RF amplifier circuit (Q505) via the band switching diode (D67).

The 1.9 MHz–14.995 MHz signals pass through the band switching diode (D65) and band-pass filter (C522–C531, L85–L87, L91), and are then applied to the RF amplifier circuit (Q505) via the band switching diode (D70).

The 15 MHz–29.995 MHz signals pass through the band switching diode (D63) and high-pass filter (C516–C520, L83, L84) and are then applied to the RF amplifier circuit (Q505) via the band switching diode (D64).

(2) 118 MHz–174.995 MHz, 330 MHz–832.995 MHz
RF signals (118 MHz–174.995 MHz, 330 MHz–832.995 MHz) from an antenna switching diode (D75) are passed through each bandpass filter and RF amplifier, and are then applied to the 1st mixer circuit (IC1) via the band switching diode (D71) and RF amplifier (IC11).

The 118 MHz–174.995 MHz signals pass through the band switching diode (D74) and low-pass filter (C8–C13, C67, C416, L14, L57–L59, L70), and are then amplified at RF amplifier (Q14). The amplified signal passes through the tunable band-pass filters (D1, D2) and band switching diode (D25).

The 330 MHz–469.995 MHz signals are amplified at RF amplifier (Q35) via the band switching diode (D3) and bandpass filter (C19–C23, C216, L2–L5). The amplified signal passes through the tunable band-pass filters (D3, D4) and band switching diode (D29).

The 470 MHz–832.995 MHz signals are amplified at RF amplifier (Q24) via the band-pass filter (C32, C33, C35–C37, C39, C144, C145), between the band switching diode (D11, D32).

(3) 30–117.995 MHz, 175–329.995 MHz
The 30 MHz–117.95 MHz, 175 MHz–329.995 MHz signals pass through the low-pass filter (C40–C43, C665, C666, L9, L10, L92), and are then applied to the RF amplifier (Q36). The amplified signals are amplified at the RF amplifier (IC11) via band switching diodes (D34, D71). The amplified signals are applied to the 1st mixer circuit (IC1).

(4) 833 MHz–1309.995 MHz
The 833 MHz–1309.995 MHz signals pass through the bandpass filter (C5, C45–C51, L11–L13, L43), and are then applied to the RF amplifier (Q26). The amplified signals are amplified at the RF amplifier (IC11) via band switching diodes (D36). The amplified signals are applied to 1st mixer circuit (IC1).

4-1-3 1ST MIXER CIRCUIT (RF UNIT)
The 1st mixer circuit converts the received RF signals to a fixed frequency of the 1st IF signal with a PLL output frequency. By changing the PLL frequency, only the desired frequency will pass through the bandpass filters at the next stage of the 1st mixer.

The filtered RF signals are mixed with 1st LO signals at the 1st mixer circuit (IC1) to produce a 266.7 MHz 1st IF signal. The 1st IF signal is from pin 6, and passed through the bandpass filter (F11) to suppress unwanted harmonic components. The filtered 1st IF signal is applied to the 2nd mixer circuit.

The 1st LO signals are generated at the 1st VCO (Q28, Q30, D45) and are applied to the 1st mixer (IC1, pin 3) directly or passing through the doubler circuit (Q31) after being amplified at the buffer amplifiers (IC4, Q40).

4-1-4 1ST IF AND 2ND MIXER CIRCUITS (RF UNIT)
The 2nd mixer circuit converts the 1st IF signal to a 2nd IF signal.

The filtered 266.7 MHz 1st IF signal from the bandpass filter is mixed with the 2nd LO signal at the 2nd mixer circuit (IC10, pin 1) to produce a 19.65 MHz 2nd IF signal. The 2nd IF signal pass through (except WFM mode) or bypass (WFM mode) the bandpass filter (F13), and is then amplified at the 2nd IF amplifier (Q5). The amplified signal is applied to the demodulator circuit.

4-1-5 DEMODULATOR CIRCUITS (RF UNIT)
The demodulator circuit converts the 2nd IF signal into AF signals.

The 19.65 MHz 2nd IF signal from the 2nd IF amplifier (Q5) is applied to the 3rd mixer section of the FM IF IC (IC2, pin 16) and is then mixed with the 3rd LO signal for conversion into a 450 kHz 3rd IF signal.
IC2 contains the 3rd mixer, limiter amplifier, quadrature detector and S-meter detector, etc. A frequency from the PLL reference oscillator is used for the 3rd LO signal (19.20 MHz).

(1) FM mode
The 3rd IF signal is output from FM IF IC (IC2, pin 3) and passes through the ceramic bandpass filter (F12). The filtered signal is fed back and amplified at the limiter amplifier section (pin 5), then demodulated AF signals at the quadrature detector section (pins 10, 11) and detector coil (L21). The demodulated AF signals are output from pin 9 and are applied to the AF circuit (LOGIC unit).

(2) WFM mode
The 3rd IF signal from the 3rd mixer bypasses the ceramic filter (F12) and fed back to the limiter amplifier section (pin 5). The amplified signal is demodulated at the quadrature detector section (pins 10, 11) and detector coil (L21). The AF signals are output from pin 9 and are applied to the AF circuit (LOGIC unit).

By connecting R55 to R54 in parallel, the output characteristics of pin 12, “RSSI”, change gradually. Therefore, the FM IF IC can detect WFM components.

(3) AM mode
The filtered 3rd IF signal from the bandpass filter (F12) is amplified at the 3rd IF amplifier (Q1). The amplified IF signal is applied to the AM detector circuit (Q4) to converted into AF signals, and the signals are applied to the AF circuit (LOGIC unit).

4-1-6 AF AMPLIFIER CIRCUIT (LOGIC UNIT)
The AF amplifier circuit amplifies the demodulated AF signals to drive a speaker.

While in FM mode, AF signals from the demodulator circuit (RF unit) are passed through the de-emphasis circuit (R118, C66, C68) with frequency characteristics of −6 dB/octave, and are then applied to the pre-amplifier (Q31) via the bandpass filter (Q30).

While in AM mode, AF signals are pass through the bandpass filter and are then applied to the pre-amplifier (Q31).

While in WFM mode, AF signals are applied to the pre-amplifier (Q31) directly.

The pre-amplified AF signals pass through the AF mute circuit (Q37) and are then applied to the electronic volume control circuit (IC14, pin 6). The level controlled AF signals are output from pin 7 and applied to the AF power amplifier (IC15, pin 1) via the buffer amplifier (Q36). The power amplified AF signals are applied to the internal speaker via the [EXT SP] jack.

The electronic volume control circuit controls AF gain, therefore, the AF output level is according to the [VOL] setting and also the squelch conditions.

4-1-7 SQUELCH CIRCUIT (LOGIC AND RF UNITS)
• NOISE SQUELCH
The noise squelch circuit cuts out AF signals when no RF signals are received. By detecting noise components in the AF signals, the squelch circuit switches the AF mute switch.

A portion of the AF signals from the FM IF IC (RF unit; IC2, pin 9) are applied to the active filter section (IC2, pin 8). The active filter section amplifies and filters noise components.

The filtered signals are applied to the noise detector section and output from IC2 (pin 13) as the “SDET” signal.

The “SDET” signal from IC2 (pin 13) passes through the noise detector (LOGIC unit; IC1), and is then applied to the CPU (LOGIC unit; IC11, pin 12) via the “SQL” line. The CPU analyzes the noise condition and outputs the “AMUTE” signal to the AF mute switch (Q37).

Even when the squelch id closed, the AF mute switch (Q37) opens at the moment of emitting beep tones.

• 2nd IF AND DEMODULATOR CIRCUITS
• TONE SQUELCH
The tone squelch circuit detects AF signals and opens the squelch only when receiving a signal containing a matching subaudible tone (CTCSS). When tone squelch is in use, and a signal with a mismatched or no subaudible tone is received, the tone squelch circuit mutes the AF signals even when noise squelch is open.

A portion of the AF signals from the FM IF IC (IC2, pin 9) passes through the low-pass filter (LOGIC unit; IC9) via the “WFMS” line to remove AF (voice) signals and is applied to the CTCSS decoder inside the CPU (LOGIC unit; IC11, pin 8) via the “RTONE” line to control the AF mute switch.

4-2 PLL CIRCUITS
4-2-1 PLL CIRCUIT (RF UNIT)
A PLL circuit provides stable oscillation of the receive 1st/2nd LO frequencies. The PLL circuit compares the phase of the divided VCO frequency to the reference frequency. The PLL output frequency is controlled by the divided ratio (N-data) of a programmable divider.

An oscillated signal from the 1st VCO passes through the buffer amplifiers (IC4, Q43) is applied to the PLL IC (IC3, pin 19) and is prescaled in the PLL IC based on the divided ratio (N-data). The PLL IC detects the out-of-step phase using the reference frequency and outputs it from pin 13. The output signal is passed through the loop filter (Q2, Q45) and is then applied to the 1ST VCO circuit as the lock voltage.

4-2-2 REFERENCE OSCILLATOR CIRCUIT
(RF UNIT)
The reference oscillator circuit (X1, IC3) generates a 19.2 MHz reference frequency which is stabilized within the temperature range –10°C (+14°F) to +60°C (+140°F). The reference frequency is applied to the PLL IC (IC3, pin 16) and the signal is output from the pin 17, and is then applied to the FM IF IC (IC2, pin 2) via the low-pass fileret.

• PLL circuit

4-2-3 1ST VCO CIRCUIT (RF UNIT)
The oscillated signal is applied to the buffer amplifiers (IC4, Q40). The amplified signal is applied to the 1st mixer circuit (IC1) via the RX LO switch circuit (D42–D44) and doubler circuit (Q31).

The 1st VCO circuit (Q28, Q30, D54) oscillates 267.2 MHz–380 MHz and 380 MHz–550 MHz by switching the SHIFT switch (Q29) “High” and “Low” respectively.

A portion of the signal from IC4 is amplified at the buffer amplifier (Q43) and is then fed back to the PLL IC (IC3, pin 2) as the comparison signal.

4-2-4 2ND VCO CIRCUIT (RF UNIT)
The 2nd LO circuit generates the 2nd LO frequencies, and the signals are applied to the 2nd mixer circuit.

The 2nd VCO circuit (Q6, L45, C80, C207, C208) oscillates 260 MHz. The oscillated signal is applied to the 2nd mixer (IC10, pin 3), and is then mixed with the 1st IF signal.

An oscillated signal from the 2nd VCO passes through the low-pass filter (C154, C250–C252, L69), and is applied to the PLL IC (IC3, pin 2), and is then output from pin 8.

• 2nd LO VCO circuit
### 4-3 POWER SUPPLY CIRCUITS

#### VOLTAGE LINE

<table>
<thead>
<tr>
<th>LINE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>BATT</td>
<td>The voltage from the attached battery.</td>
</tr>
<tr>
<td>VP</td>
<td>Common 13 V converted from BATT line by the DC-DC convertors (IC10 and D3, D5, D15). The output voltage is applied to the PLL circuit (RF unit).</td>
</tr>
<tr>
<td>R3V</td>
<td>Receive 3V controlled by the R3V regulator circuit (Q4) using the “RX” signal from CPU (IC11).</td>
</tr>
<tr>
<td>+3S</td>
<td>Common 3V converted by the +3S regulator circuit (Q3, Q39) using the “+3SC” signal from CPU (IC11).</td>
</tr>
<tr>
<td>+3V</td>
<td>Common 3V converted by the +3V regulator circuit (Q6) using the “POWERC” signal from CPU (IC11).</td>
</tr>
<tr>
<td>Pin number</td>
<td>Port name</td>
</tr>
<tr>
<td>------------</td>
<td>-----------</td>
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<tr>
<td>26</td>
<td>LIGHT</td>
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<td>PSTB</td>
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<td>47</td>
<td>PDA</td>
</tr>
<tr>
<td>48</td>
<td>DBL2</td>
</tr>
<tr>
<td>50</td>
<td>300MC</td>
</tr>
<tr>
<td>51</td>
<td>GC</td>
</tr>
<tr>
<td>52</td>
<td>800MC</td>
</tr>
<tr>
<td>53</td>
<td>UHFC</td>
</tr>
<tr>
<td>54</td>
<td>VHFC</td>
</tr>
<tr>
<td>55</td>
<td>SHIFT</td>
</tr>
<tr>
<td>56</td>
<td>HFC</td>
</tr>
</tbody>
</table>
SECTION 5  ADJUSTMENT PROCEDURES

5-1 PREPARATION
The receiver (IC-R2) must be adjusted on the adjustment mode after programmed adjustment frequency data into memory channel. When you program adjustment frequency data into memory channel, optional CS-R2 PROGRAMMING SOFTWARE, OPC-478 CLONING CABLE are required.

■ REQUIRED TEST EQUIPMENT

<table>
<thead>
<tr>
<th>EQUIPMENT</th>
<th>GRADE AND RANGE</th>
<th>EQUIPMENT</th>
<th>GRADE AND RANGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC power supply</td>
<td>Output voltage: 3.0 V DC</td>
<td>Frequency counter</td>
<td>Frequency range: 0.1–600 MHz</td>
</tr>
<tr>
<td></td>
<td>Current capacity: 1 A or more</td>
<td></td>
<td>Frequency accuracy: ±1 ppm or better</td>
</tr>
<tr>
<td>AC millivoltmeter</td>
<td>Measuring range: 10 mV–10 V</td>
<td></td>
<td>Sensitivity: 100 mV or better</td>
</tr>
<tr>
<td>External speaker</td>
<td>Input impedance: 8 Ω</td>
<td></td>
<td>Standard signal generator (SSG)</td>
</tr>
<tr>
<td></td>
<td>Capacity: 1 W or more</td>
<td></td>
<td>Frequency range: 0.1–1300 MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Output level: 0.1 µV–32 mV (~127 to –17 dBm)</td>
</tr>
</tbody>
</table>

■ SOFTWARE INSTALLATION

NOTE: Before using the program, make a backup copy of the original disk. After making a backup copy, keep the original disk in a safe place.

1. Boot up DOS.
2. Insert the backup disk into the floppy drive A.
3. Type the following to install the adjustment program:
   A:\>INSTALL A:C\CSR2 [Enter]

■ ADJUSTMENT FREQUENCY DATA

When program adjustment frequency data (at right) into memory channel, back up the original memory data using the optional CS-R2, OPC-478, and re-program it after adjustment.

CAUTION: When clone the adjustment frequency data to the receiver, the receiver's memory channel will be overwritten the data and deleted original memory data at same time.

■ ENTERING THE ADJUSTMENT MODE

1. Connect a JIG (see illustration at CONNECTION) to the [SP] jack.
2. Push and hold [FUNC], then turn power ON.
3. Disconnect the JIG and connect a PC with an OPC-478.
4. Boot up DOS.
5. Type the following to start up the adjustment program:
   C:\>CD CSR2 [Enter]
   C:\>CSR2 [Enter]
   • Main menu appears at the top side of the cloning program, select the sub-menu “Screen”–“Memory CH”–“Bank 1”, then input adjustment frequency (at right).
   • Application writes adjustment frequency data to the connected receiver.
7. Disconnect the cloning cable and turn power OFF, then turn power ON to start adjustment.

■ OPERATING ON THE ADJUSTMENT MODE

Change the value: [DIAL]
Change the channel [UP]: [BAND]
Change the channel [DOWN]: [BAND]

■ EXITING THE ADJUSTMENT MODE

When the adjustment is finished, the receiver must be cancelled adjustment mode to use normal operation, otherwise receiver does not work properly.

1. Turn power OFF.
2. Push and hold [FUNC] and [V/M], then turn power ON.

NOTE: All memory data except adjustment value will be cleared at this operation.
DC power supply 3.0 V/1.0 A

Terminator for the entering adjustment mode

68 kΩ

Standard signal generator

AD-92SMA
Optional SMA–BNC adaptor

1/8" (3.5 mm) 3-conductor plug

to [SP] jack
## 5-2 PLL ADJUSTMENT

<table>
<thead>
<tr>
<th>ADJUSTMENT</th>
<th>ADJUSTMENT CONDITION</th>
<th>MEASUREMENT</th>
<th>VALUE</th>
<th>ADJUSTMENT POINT</th>
</tr>
</thead>
<tbody>
<tr>
<td>1ST VCO LOCK VOLTAGE (SHIFT ON)</td>
<td></td>
<td>RF</td>
<td>1.9 V – 2.9 V</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>less than 12 V</td>
<td>Verify</td>
</tr>
<tr>
<td>1 • Displayed frequency : 493.300 MHz</td>
<td>Receiving</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2 • Displayed frequency : 282.900 MHz</td>
<td>Receiving</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(SHIFT OFF)</td>
<td></td>
<td>RF</td>
<td>1.4 V – 2.4 V</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>less than 12 V</td>
<td></td>
</tr>
<tr>
<td>1 • Displayed frequency : 0.495 MHz</td>
<td>Receiving</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2 • Displayed frequency : 493.295 MHz</td>
<td>Receiving</td>
<td></td>
<td></td>
<td></td>
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<td>2ND VCO LOCK VOLTAGE</td>
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<td>RF</td>
<td>0.4 V – 1.0 V</td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td>less than 2.5 V</td>
<td></td>
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<td>1 • Displayed frequency : 430.000 MHz</td>
<td>Receiving</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2 • Displayed frequency : 493.300 MHz</td>
<td>Receiving</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>REFERENCE FREQUENCY</td>
<td></td>
<td>RF</td>
<td>546.7999 MHz – 546.8001 MHz</td>
<td>LOGIC [DIAL]</td>
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<tr>
<td></td>
<td>(FR ch) 280.100 MHz</td>
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<tr>
<td>DETECTOR OUTPUT VOLTAGE</td>
<td></td>
<td>RF</td>
<td>1.0 V</td>
<td></td>
</tr>
<tr>
<td></td>
<td>(tk ch) 145.600 MHz</td>
<td></td>
<td></td>
<td>L21</td>
</tr>
<tr>
<td>1 • Displayed frequency :</td>
<td>Receiving</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>145.600 MHz</td>
<td>Connect an SSG to the antenna connector and set as:</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1 • Connect an SSG to the antenna connector and set as:</td>
<td>Level : 1 mV* (60 dBµ)</td>
<td>RF</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2 • Deviation : ± 3.5 kHz</td>
<td>Receiving</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3 • Modulation : 1 kHz</td>
<td>Receiving</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

*This output level of the standard signal generator (SSG) is indicated as SSG's open circuit.*
L21
Detector output voltage adjustment

QUAD
Detector output voltage check point

LV2
2nd VCO lock voltage check point

F
PLL Reference Frequency check point

LV1
1st VCO lock voltage check point
**5-3 RECEIVER ADJUSTMENT**

<table>
<thead>
<tr>
<th>ADJUSTMENT</th>
<th>ADJUSTMENT CONDITION</th>
<th>MEASUREMENT</th>
<th>VALUE</th>
<th>ADJUSTMENT POINT</th>
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<tbody>
<tr>
<td><strong>VHF SENSITIVITY</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
| 1 | • Displayed frequency : (tk ch) 145.600 MHz  
• Connect an SSG to the antenna connector and set as :  
  Level : 1 µV* (~107 dBm)  
  Modulation : 1 kHz  
  Deviation : ±3.5 kHz  
• Receiving | RF | Connect the DC voltmeter to the check point SEN. | Maximum DC voltage | LOGIC | [DIAL] |
| **UHF SENSITIVITY** | | | | |
| 1 | • Displayed frequency : (tk ch) 435.600 MHz  
• Connect an SSG to the antenna connector and set as :  
  Level : 1 µV* (~107 dBm)  
  Modulation : 1 kHz  
  Deviation : ±3.5 kHz  
• Receiving | RF | Connect the DC voltmeter to the check point SEN. | Maximum DC voltage | LOGIC | [DIAL] |
| **S-METER** | | | | |
| 1 | • Displayed frequency : (RS ch) 14.100 MHz  
• Connect the SSG to the antenna connector and set as :  
  Level : 0.5 µV* (~113 dBm)  
  Modulation : 1 kHz  
  Deviation : ±3.5 kHz  
• Receiving | | | | Push and hold the [MOD] key.  
• Verify that S-Meter shows S4 (3dots). |
| 2 | • Displayed frequency : (RS ch) 145.100 MHz  
• Set the SSG as :  
  Level : 0.5 µV* (~113 dBm)  
• Receiving | | | | |
| 3 | • Displayed frequency : (RS ch) 200.100 MHz  
• Set the SSG as :  
  Level : 0.5 µV* (~113 dBm)  
• Receiving | | | | |
| 4 | • Displayed frequency : (RS ch) 435.100 MHz  
• Set the SSG as :  
  Level : 0.5 µV* (~113 dBm)  
• Receiving | | | | |
| 5 | • Displayed frequency : (RS ch) 650.100 MHz  
• Set the SSG as :  
  Level : 0.5 µV* (~113 dBm)  
• Receiving | | | | |
| 6 | • Displayed frequency : (RS ch) 1100.100 MHz  
• Set the SSG as :  
  Level : 1 µV* (~107 dBµ)  
• Receiving | | | | |

*This output level of the standard signal generator (SSG) is indicated as SSG’s open circuit.
SEN
VHF and UHF sensitivity check point.
# SECTION 6 PARTS LIST

## [LOGIC UNIT]

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<td>S.I.C</td>
<td>HD74LV00TELL</td>
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<td>1130009020</td>
<td>S.I.C</td>
<td>X25650S8I-2.5T6</td>
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<tr>
<td>1180001820</td>
<td>S.I.C</td>
<td>XC62FFP3002MR</td>
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<td>1180001720</td>
<td>S.I.C</td>
<td>S-81332H3-KC-T1</td>
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<td>111004620</td>
<td>S.I.C</td>
<td>S-8072SS-AN-T1</td>
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<td>111003880</td>
<td>S.I.C</td>
<td>NJM2904-TE1</td>
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<td>111004780</td>
<td>S.I.C</td>
<td>XC6371AS1PR</td>
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<td>S.I.C</td>
<td>M38267ML-216GP [USA] only</td>
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<td>1140007720</td>
<td>S.I.C</td>
<td>M38267ML-222GP other</td>
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<td>1190000710</td>
<td>S.I.C</td>
<td>TA1056F (TP1)</td>
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<table>
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<td>DT414EE TL</td>
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<td>1590001780</td>
<td>S.TRANSISTOR</td>
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<td>1530002280</td>
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<td>2SC4081 T107 S</td>
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<td>FET 2SJ144-Y (TE85R)</td>
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<td>2SC4081 T107 S</td>
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<td>2SA1588-GR (TE85R)</td>
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<td>S.TRANSISTOR</td>
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<td>S.DIODE</td>
<td>1S372 (TE85R)</td>
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<tr>
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<td>S.DIODE</td>
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<td>S.DIODE</td>
<td>MA132WK(TX)</td>
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<td>S.DIODE</td>
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<tbody>
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<td>6050010310</td>
<td>S.XTAL</td>
<td>CR-613 (4.935 MHz)</td>
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<td>6200008630</td>
<td>S.COIL</td>
<td>CD54-101KC</td>
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## [LOGIC UNIT]

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<td>R3</td>
<td>7030005240</td>
<td>S.RESISTOR</td>
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S. = Surface mount
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<td>S.DIODE</td>
<td>ELJRE 33NG-F</td>
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<td>ELJRE 6NG-F</td>
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<td>FL-293 (19.650 MHz)</td>
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<td>S.XTAL</td>
<td>CR-593 (19.200 MHz)</td>
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**[RF UNIT]**

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<td>L4</td>
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### 7-1 CABINET PARTS

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**Screw abbreviations**

A, B0, BT: Self-tapping  
PH: Pan head  
FH: Flat head  
BiH: Bind head  
NI: Nickel  
SUS: Stainless  
ZK: Black
UNIT abbreviation: (C): CHASSIS PARTS, (R): RF UNIT, (L): LOGIC UNIT
### Section 8  Semi-Conductor Information

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SECTION 9  BOARD LAYOUTS

9 - 1 LOGIC UNIT

- TOP VIEW
SECTION 11  VOLTAGE DIAGRAM

• LOGIC UNIT

[Diagram of the Logic Unit]
Icom Inc.
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Fax : 06 6793 0013
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