2.9 GHz PLL for SAT TV Tuner with UNi-Bus

Description

The U6239B is a single-chip frequency synthesizer with bidirectional I²C bus control and unidirectional 3-wire bus control, developed for SAT TV-tuner and cable tuner applications.

This IC contains an integrated preamplifier, a high frequency prescaler, a reference divider with multiple programmable divider ratios, a crystal oscillator, a phase/ frequency detector together with a charge pump, a tuning amplifier and an analog-to-digital converter.

Features

- 2.9 GHz divide-by-16 prescaler integrated
- UNi-BUS:
  I²C bus and 3-wire bus
  I²C bus software compatible to U6223B
  3-wire bus software compatible to LC7215 (Sanyo)
- I²C bus mode:
  4 bidirectional ports (open collector)
  2 unidirectional ports (open collector)
  5 level ADC or unidirectional port (open collector)
  Address mode select function (AMS, Pin 3):
  3 or 4 addresses selectable via Pin 10
- 3-wire bus mode:
  4 unidirectional ports (open collector)
  Lock output (open collector)
- Programmable reference divider
- Low power consumption (typ. 5 V / 23 mA)
- Electrostatic protection according to MIL-STD 883

Block Diagram

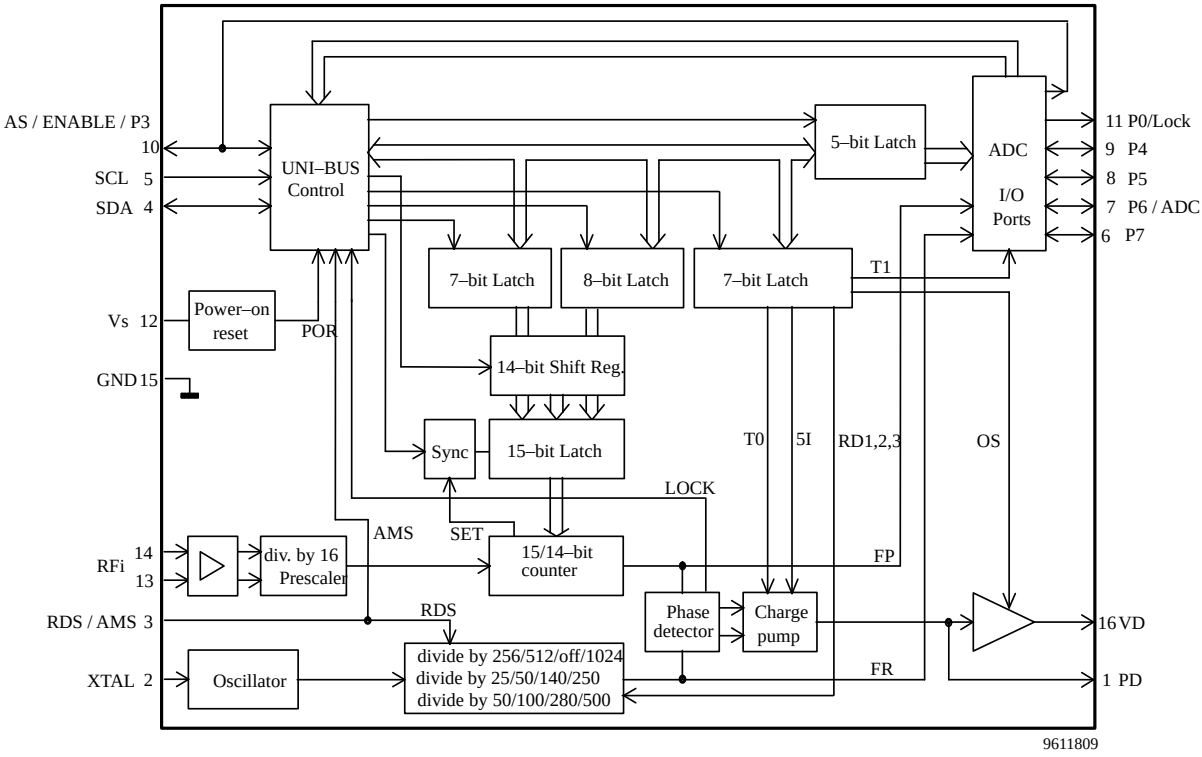
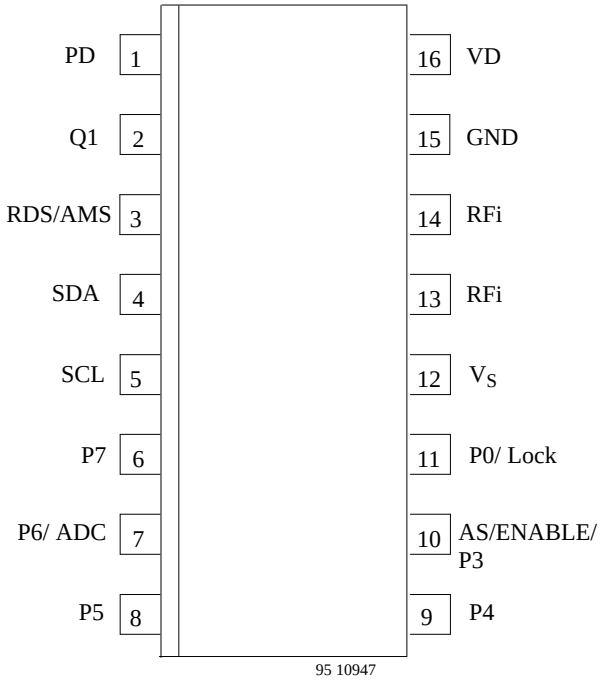


Figure 1.

Ordering Information

Extended Type Number	Package	Remarks
U6239B-AFPG3	SO16, plastic package	Taped and reeled
		SSO16 package on request

Pin Configuration



Pin	Symbol	Function
1	PD	Charge pump output
2	Q1	Crystal input
3	RDS/ AMS	Reference divider select input (3-wire bus mode) Address mode select input (I^2C bus mode)
4	SDA	Data input/ output
5	SCL	Clock input
6	P7	Port 7 input/ output
7	P6/ ADC	Port 6 output Analog-Digital-Converter input
8	P5	Port 5 input/ output
9	P4	Port 4 input/ output
10	AS/ ENABLE/ P3	Address select input Enable input Port 3 output
11	P0/Lock	Port 0 output/Lock output
12	V_S	Supply voltage
13	RFi	RF input
14	RFi	RF input
15	GND	Ground
16	VD	Active filter output

Circuit Description

The U6239B is a single-chip PLL designed for SAT TV tuner and cable tuner. It consists of a divide-by-16 prescaler with an integrated preamplifier, a 15-bit programmable divider, a crystal oscillator, and a reference divider with selectable divider ratios, a phase/ frequency detector together with a charge pump which drives the tuning amplifier. Only one external transistor is required for varactor line driving. The device can be controlled via I^2C bus format or via 3-wire bus format. It detects automatically which bus format has been received. Therefore, there is no need for a bus selection pin. In I^2C bus mode, the device has four programmable or one fixed and three programmable I^2C bus addresses, depending on the voltage level at Pin 3. They are programmed by applying a specific input voltage to the address select input Pin 10, enabling the use of up to four synthesizers in a system. If the fixed address is used, this pin can be used as a normal output port. The same pin serves as the enable signal input in 3-wire bus mode. Depending whether the fixed address is used or not there are five or six open collector outputs for switching functions available. In 3-wire bus mode there are four open collector outputs and one lock signal output. All open collector outputs are capable of sinking at least 10 mA. In I^2C bus mode an analog-to-digital converter (ADC) is available for digital AFC (automatic frequency control) applications and the ports P4, P5 and P7 can also be used as input ports.

Functional Description

The U6239B is programmed via a 2-wire I^2C bus or 3-wire bus depending on the received data format. In I^2C bus mode the three bus input pins 4, 5, 10 are used as SDA, SCL and address select inputs or in 3-wire bus mode as date, clock and enable inputs, respectively. The data include the scaling factor SF and port output information. In I^2C bus mode there are some additional functions available (ADC, bidirectional ports, etc.)

Oscillator frequency calculation :

$$\mathbf{f_{VCO} = 16 \times SPF \times f_{refosc}/SRF}$$

f_{vco}: Locked frequency of voltage controlled oscillator

SPF : Scaling factor of programmable divider (15 bit in I^2C bus mode, 14 bit in 3-wire bus mode)

SRF : Scaling factor of reference divider (÷ 25/ ÷ 50/ ÷ 140/ ÷ 250/ ÷ 256/ ÷ 512/ ÷ 1024 in I^2C bus mode, ÷ 25/ ÷ 50/ ÷ 100/ ÷ 140/ ÷ 250 ÷ 280/ ÷ 500 in 3-wire bus mode)

f_{refosc}: Reference oscillator frequency: 3.2/ 4 MHz crystal or external reference frequency (max. 8 MHz)

The input amplifier together with a divide-by-16 prescaler provides excellent sensitivity (see “Typical prescaler input sensitivity”). The input impedance is shown in the diagram “Typical input impedance”. When a new divider ratio is entered according to the requested f_{VCO}, the phase detector and charge pump adjusts the control voltage of the VCO together with the tuning amplifier until the output signals of the programmable divider and the reference divider are in frequency locked and phase locked. The reference frequency may be provided by an external source, capacitively coupled into Pin 2, or by using an on-board crystal with an 18 pF capacitor in series. The crystal operates in the series resonance mode. The reference divider division ratio is selectable to ÷ 25/ ÷ 50/ ÷ 140/ ÷ 250/ ÷ 256/ ÷ 512/ ÷ 1024 in the I^2C bus mode and ÷ 25/ ÷ 50/ ÷ 100/ ÷ 140/ ÷ 250/ ÷ 280/ ÷ 500 in the 3-wire bus mode.

In I^2C bus mode, the division ratio may be set via three bits, in 3-wire bus mode via two bits and a voltage at the reference divider select input Pin 3. In addition, there are port outputs available for band switching and other purposes.

Application

A typical application is shown on page 14. All input/ output interface circuits are shown on the pages 12 and 13. Some special features which are related to test- and alignment procedures for tuner production are explained together with the bus mode descriptions.

Absolute Maximum Ratings

All voltages are referred to GND (Pin 15)

Parameters		Symbol	Conditions	Min.	Max.	Unit
Supply voltage	Pin 12	Vs		–0.3	6	V
RF input voltage	Pins 13, 14	RFi		–0.3	Vs + 0.3	V
Port output current	Pins 6-11	P0, P3-7	Open collector	–1	15	mA
Total port output current	Pins 6-11	P0, P3-7	Open collector	–1	50	mA
Port input/ output voltage	Pins 6-10	P3-7	In off state	–0.3	14	V
Port output voltage	Pins 6-11	P0, P3-7	In on state	–0.3	6	V
Bus input/ output voltage	Pins 4 and 5	VSDA, VSCL		–0.3	6	V
SDA output current	Pin 4	ISDA	Open collector	–1	5	mA
Address select/ Enable input Port output voltage	Pin 10	AS/ ENABLE/ P3	Port in off state	–0.3	14	V
Charge pump output voltage	Pin 1	PD		–0.3	Vs + 0.3	V
Active filter output voltage	Pin 16	VD		–0.3	Vs + 0.3	V
Crystal oscillator voltage	Pin 2	Q1		–0.3	Vs + 0.3	V
Reference divider select input/ Address mode select input	Pin 3	RDS/ AMS		–0.3	V_S + 0.3	V
Junction temperature		T_j		–40	125	°C
Storage temperature		T_{stg}		–40	125	°C

Operating Range

All voltages are referred to GND (Pin 15)

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	Pin 12	V_S	4.5	5	5.5	V
Ambient temperature		T_{amb}	–20		85	°C
Input frequency	Pins 13 and 14	RFi	250		2900	MHz
Programmable divider	I^2C bus mode	SF	256		32767	
Programmable divider	3-wire bus mode	SF	256		16383	

Thermal Resistance

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Junction ambient	Package SO16 soldered to PCB	R_{thJA}		110		K/W

Electrical Characteristics

Test conditions (unless otherwise specified): V_S = 5 V, T_{amb} = 25°C

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Supply current (prescaler on)	Ports off Pin 12	ICC		23		mA
Input sensitivity						
f_{RFi} = 250 MHz	Pin 13	Vi [1])	100		300	mV_{rms}
f_{RFi} = 750 -2900 MHz	Pin 13	Vi [1])	20		300	mV_{rms}
Crystal oscillator						
Recommended crystal series resistance			10		200	Ω
Crystal oscillator drive level	Pin 2			50		mV_{rms}
Crystal oscillator source impedance	Nominal spread ± 15% Pin 2			–650		Ω
External reference input frequency	AC coupled sinewave Pin 2		2		8	MHz
External reference input amplitude	AC coupled sinewave Pin2		70		200	mV_{rms}
Port outputs (current limited, output function only in I^2C bus mode) Port P0 at Pin 11. Port P3 at Pin 10, is only usable with AMS = 'L' (= 3 address mode).						
P0, P3 Sink current	VH = 12 V, Pins 10 and 11	ISL	0.7	1	1.5	mA
Leakage current	VH = 13.2 V	IL			10	µA
Port outputs, Lock output (open collector, locked = 'L'. Ports P4 – P7 at Pins 6–9) Lock output at Pin 11, only in 3-wire bus mode.						
Saturation voltage	IL = 10 mA	VSL [2])			0.5	V
Leakage current	VH = 13.2 V	IL			10	µA
Port inputs (Ports 4, 5 and 7 at Pins 6, 8 and 9)						
Input voltage high		Vi 'H'	2.7			V
Input voltage low		Vi 'L'			0.8	V
Input current high	Vi 'H' = 13.2 V	Ii 'H'			10	µA
Input current low	Vi 'L' = 0 V	Ii 'L'	–10			µA

Electrical Characteristics (continued)

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
ADC input (ADC, Pin 7, see page 8 for ADC-levels)						
Input current high	Vi 'H' = 13.2 V	Ii 'H'			10	µA
Input current low	Vi 'L' = 0 V	Ii 'L'	–10			µA
Charge pump output (PD)						
Charge pump current 'H'	5I = 1, VPD = 1.7 V, Pin 1	IPDH		± 180		µA
Charge pump current 'L'	5I = 0, VPD = 1.7 V, Pin 1	IPDL		± 50		µA
Charge pump leakage current	T0 = 1, VPD = 1.7 V, Pin 1	IPDTRI		± 5		nA
Charge pump amplifier gain	Pins 1 and 16			6400		
Bus inputs Data and Clock (SDA, SCL) I^2C bus mode and 3-wire bus mode						
Input voltage high	Pins 4 and 5	Vi 'H'	3		5.5	V
Input voltage low	Pins 4 and 5	Vi 'L'			1.5	V
Input current high	Vi 'H' = V_S, Pins 4 and 5	Ii 'H'			10	µA
Input current low	Vi 'L' = 0 V, Pins 4 and 5	Ii 'L'	–20			µA
Output voltage SDA (open collector)	ISDA'L' = 3 mA, Pin 4	VSDA 'L'			0.4	V
Bus input Enable, 3-wire bus mode (ENABLE, Pin 10)						
Input voltage high	Pin 10	Vi 'H'	75% V_S		V_S + 0.3 V	V
Input voltage low	Pin 10	Vi 'L'			1.0	V
Input current high	Vi 'H' = V_S, Pin 10	Ii 'H'			10	µA
Input current low (RDS = 'L')	Vi 'L' = 0 V, Pin 10	Ii 'L'	–10			µA
Input current low (RDS = 'H')	Vi 'L' = 0 V, Pin 10	Ii 'L'	–100			µA
Address selection / port output (AS/P3, Pin 10)						
Input current low (AMS = L)	Vi 'L' = 0 V (3 address)	Ii 'L'	–10			µA
Input current high (AMS = L)	Vi 'H' = 13.2 V (3 address)	Ii 'H'			10	µA
Input current low (AMS = H)	Vi 'L' = 0 V (4 address)	Ii 'L'	–100			µA
Input current high (AMS = H)	Vi 'H' = V_S (4 address)	Ii 'H'			10	µA
Reference divider select/Address mode select (RDS, AMS)						
Input voltage high	Pins 4 and 5	Vi 'H'	3		5.5	V
Input voltage low	Pins 4 and 5	Vi 'L'			1.5	V
Input current high	Vi 'H' = V_S, Pins 4 and 5	Ii 'H'			10	µA
Input current low	Vi 'L' = 0 V, Pins 4 and 5	Ii 'L'	–20			µA

Notes:
[1]) RMS - voltage calculated from the measured available power on 50 Ω.
[2]) Tested with one port active. The collector voltage of an active port must not exceed 6 V.

I²C Bus Description

Functional Description

When the U6239B is controlled via a 2-wire I²C bus format, then data and clock signals are fed into the SDA and SCL lines respectively. Depending on the LSB of the address byte, the device can either accept new data (write mode: LSB = 0) or send data (read mode: LSB = 1).

Depending on the voltage at the address mode select input, the device has one fixed and three programmable or four programmable I²C bus addresses. The tables "I²C bus write data format" and "I²C bus read data format" describe the format of the data and show how to select the device addresses by applying the appropriate voltages at address select Pin 10 and the address mode select Pin 3.

Write Mode (Address byte LSB = 0)

When write mode is activated and the correct address byte is received, the SDA line is pulled low by the device during the acknowledge period. The SDA line is also pulled low during the acknowledge periods, when additional data bytes are programmed. After the address transmission (first byte), data bytes can be sent to the device. There are four data bytes requested to fully program the device. Once the correct address is received and acknowledged, the first bit of the following byte determines whether that byte is interpreted as byte 2 or 4; a logic 0 for divider information and a logic 1 for control and port output information. If byte 2 has been received, the device always expects byte 3 next. Likewise if byte 4 has been received, byte 5 is expected. Additional data bytes can be entered without the need to re-address the device until an I²C bus stop condition is recognized. This allows a smooth frequency sweep for fine tuning AFC purposes. The table "I²C bus pulse diagram" provides some possible data transfer examples. In addition, the stop condition is not a must, the device may be programmed by using the start condition only.

The programmable divider bytes PDB1 and PDB2 are stored in a 15-bit latch and control the division ratio of the 15-bit programmable divider. The control byte CB1 enables the controlling of the following special functions:

- 5I bit switches between low and high charge pump current
- T1 bit enables divider test mode when it is set to logic 1
- T0 bit enables the charge pump to be disabled when it is set to logic 1
- RD3, 2 and 1 - bits enable selection of the reference divider ratio
- OS-bit disables the charge pump drive amplifier output when it is set to logic 1.

The charge pump current can only be controlled in I²C bus mode. In 3-wire bus mode, the high charge pump current is always active.

The OS-bit function disables the complete PLL function. This enables the tuner alignment by supplying the tuning voltage directly through the 30 V supply voltage of the tuner. The control byte CB2 programs the port outputs P0 and P3 - 7.

Description	I²C Bus Data Format								
	MSB							LSB	
Address byte	1	1	0	0	0	AS1	AS2	0	A
Programmable divider, byte 1	0	n14	n13	n12	n11	n10	n9	n8	A
Programmable divider, byte 2	n7	n6	n5	n4	n3	n2	n1	n0	A
Control byte 1	1	5I	T1	T0	RD3	RD2	RD1	OS	A
Control byte 2	P7	P6	P5	P4	P3	X	X	P0	A

A = Acknowledge; X = not used

n0 to n14 :	Scaling factor (SF)	SF = 16384 × n14 + 8192 × n13 + ... + 2 × n1 + n0 SF - range: 256 to 32767	
T0, T1 :	Test mode selection	T1 = 1: divider test mode on, FP at Pin 6, FR at Pin 7	T1 = 0: divider test mode off
		T0 = 1: charge pump disable	T0 = 0: charge pump enable
P0, 3 to 7:	Port outputs	P0, 3, 4, 5, 6, 7 = 1: port active	
5I :	Charge pump current switch	5I = 1: high current	5I = 0: low current
OS :	Output switch	OS = 1: varicap drive disable	OS = 0: varicap drive enable

I²C Bus Description (continued)

Reference divider selection RD1, RD2, RD3:

RD3	RD2	RD1	Reference Divider Ratio	Frequency Step Size*	Max. Operating Frequency*
1	0	0	1024	62.5 kHz	2.047 GHz
1	0	1	off	–	–
1	1	0	256	250 kHz	2.9 GHz
1	1	1	512	125 kHz	2.9 GHz
0	0	0	140	457.14 kHz	2.9 GHz
0	0	1	25	2560 kHz	2.9 GHz
0	1	0	250	256 kHz	2.9 GHz
0	1	1	50	1280 kHz	2.9 GHz

* when a 4MHz crystal is used

Address selection AS1, AS2, AMS:

AMS Voltage at Pin 3	AS1	AS2	Address	Dec. Value	Voltage at Pin 10
< 0.8 V or open	0	0	C0	192	0 to 10% V_S
< 0.8 V or open	0	1	C2	194	always valid
< 0.8 V or open	1	0	C4	196	40 to 60% V_S
< 0.8 V or open	1	1	C6	198	90% V_S to 13.2 V
> 2.4	0	0	C0	192	0 to 10% V_S
> 2.4	0	1	C2	194	open
> 2.4	1	0	C4	196	40 to 60% V_S
> 2.4	1	1	C6	198	90% V_S to V_S

Read Mode (Address byte LSB = 1)

After the address transmission (first byte), the status byte can be read from the device on the SDA line (MSB first). Data is valid on the SDA line during logic high of the SCL signal. The controller accepting the data has to pull the SDA line to low-level during all status-byte acknowledge periods to read another status byte. If the controller fails to pull the SDA line to low-level during this period, the device will then release the SDA line to allow the controller to generate a STOP condition.

The POR bit (power-on-reset) is set to a logic 1 when the supply voltage V_S of the device has dropped below 3 V (at 25°C) and also when the device is initially turned on. The POR bit is reset to a logic 0 when the read sequence is terminated by a STOP condition. When the POR bit is set high (at low V_S), this indicates that all the programmed information is lost and the port outputs are all set to high impedance state.

The FL bit indicates whether the loop is in phase lock condition (logic 1) or not (logic 0).

If the ADC or the ports are to be used as inputs, the corresponding outputs must be programmed to a high impedance state (logic 1).

The bits I2, I1 and I0 show the status of the I/O ports P7, P5 and P4 respectively. A logic 0 indicates a LOW level and a logic 1 a HIGH level (TTL levels).

The bits A2, A1 and A0 represent the digital information of the 5-level ADC. This converter can be used to feed AFC information to the controller from the IF section of the receiver, as shown in the typical application circuit on page 14.

I²C Bus Description (continued)

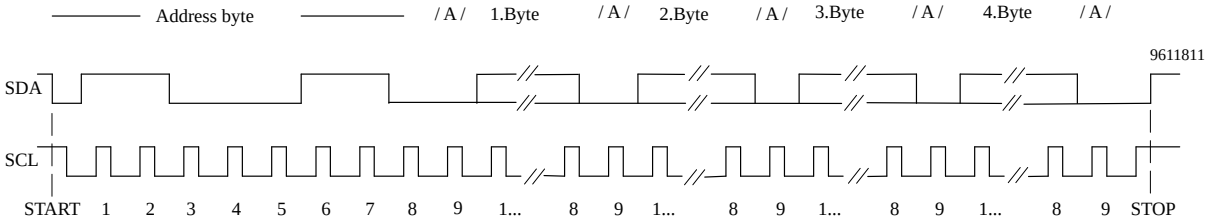
Description	I²C Bus Read Data Format								
	MSB							LSB	
Address byte	1	1	0	0	0	AS1	AS2	1	A
Status byte	POR	FL	I2	I1	I0	A2	A1	A0	–

POR : Power-on reset flag: POR = 1 on power on
FL : In-lock flag: FL = 1, when loop is phase locked
I2, I1, I0 : Digital information of I/O-ports P7, P5 and P4 respectively
A2, A1, A0 : Digital data of the 5-level ADC. see next table

A/D Converter Levels:

A2	A1	A0	Input voltage to ADC Pin 9
1	0	0	60% Vs to 13.2 V
0	1	1	45% to 60% Vs
0	1	0	30% to 45% Vs
0	0	1	15% to 30% Vs
0	0	0	0 V to 15% Vs

I²C Bus Pulse Diagram



Data transfer examples
START – ADR – PDB1 – PDB2 – CB1 – CB2 – STOP
START – ADR – CB1 – CB2 – PDB1 – PDB2 – STOP
START – ADR – PDB1 – PDB2 – CB1 – STOP
START – ADR – PDB1 – PDB2 – STOP
START – ADR – CB1 – CB2 – STOP
START – ADR – CB1 – STOP

Description
START = Start condition
ADR = Address byte
PDB1 = Programmable divider byte 1
PDB2 = Programmable divider byte 2
CB1 = Control byte 1
CB2 = Control byte 2
STOP = Stop condition

I²C Bus Description (continued)

I²C Bus Timing

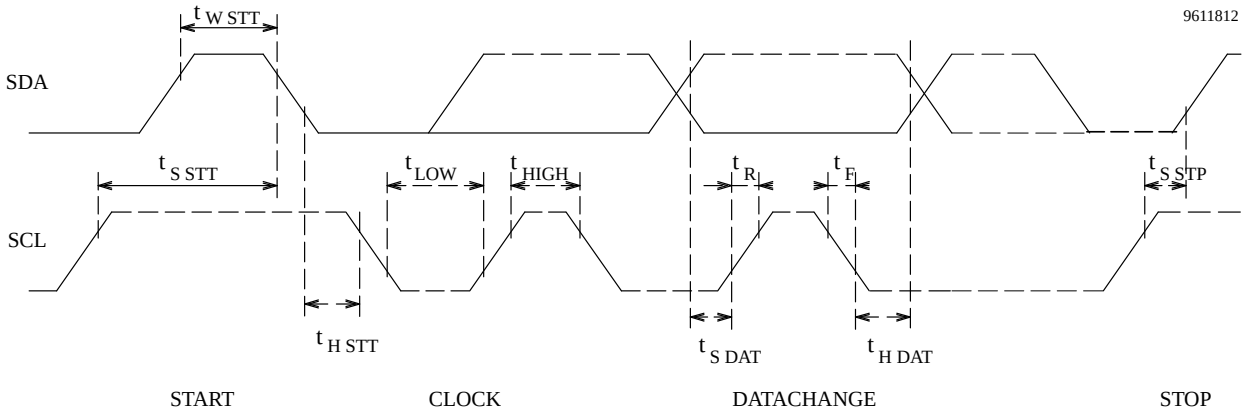


Figure 2.

Parameters	Symbol	Min.	Max.	Unit
Rise time SDA, SCL	t_R		15	µs
Fall time SDA, SCL	t_F		15	µs
Clock frequency SCL	f_{SCL}	0	100	kHz
Clock ‘H’ pulse	t_{HIGH}	1		µs
Clock ‘L’ pulse	t_{LOW}	1		µs
Hold time start	$t_{H\ STT}$	1		µs
Waiting time start	$t_{W\ STT}$	1		µs
Setup time start	$t_{S\ STT}$	1		µs
Setup time stop	$t_{S\ STP}$	1		µs
Setup time data	$t_{S\ DAT}$	0.25		µs
Hold time data	$t_{H\ DAT}$	0		µs

3-Wire Bus Description

When the U6239B is controlled via a 3-wire bus format, then data, clock and enable signals are fed into the SDA, SCL and AS/ENABLE/P3 lines respectively. The diagram “3-wire bus pulse diagram” shows the data format. The data consist of a single word which contains the programmable divider (14 bit) and port information. Bit No. 15 of the programmable divider is always zero, when the 3-wire bus mode is active. The data is only clocked into the internal data shift register on the negative clock transition during the enable high period. During enable low periods the clock input is disabled. New data words are only accepted by the internal data latches from the shift register on a negative transition of the enable signal if exactly eigtheen clock pulses were sent during the high period of the enable. The data sequence and the timing is described in the following diagrams.

In 3-wire bus mode Pin 9 automatically becomes the lock-signal output. An improved lock detect circuit generates a flag when the loop has attained lock. ‘In lock’ is indicated by a low impedance state (on) of the open collector output.

In 3-wire bus mode the high charge pump current is always active. The charge pump current can only be controlled in I²C bus mode.

The complete PLL function can be disabled by programming a normally not used division ratio of zero. This allows the tuner alignment by supplying the tuning voltage directly through the 33 V supply voltage of the tuner.

In 3-wire bus mode the division ratio of the reference divider is controlled via information RD1, RD2 and the reference divider select input Pin 3.

3-Wire Bus Description (continued)

Reference divider selection RD1, RD2, RDS:

RDS Voltage at Pin 3	RD2	RD1	Reference Divider Ratio	Frequency Step Size*	Maximum Operating Frequency*
0 to 10% V_S or open	0	0	280	228.57 kHz	2.9 GHz
0 to 10% V_S or open	0	1	50	1280 kHz	2.9 GHz
0 to 10% V_S or open	1	0	500	128 kHz	2.097 GHz
0 to 10% V_S or open	1	1	100	640 kHz	2.9 GHz
90 to 100% V_S	0	0	140	457.14 kHz	2.9 GHz
90 to 100% V_S	0	1	25	2560kHz	2.9 GHz
90 to 100% V_S	1	0	250	256 kHz	2.9 GHz
90 to 100% V_S	1	1	50	1280 kHz	2.9 GHz

* when a 4-MHz crystal is used

3-Wire Bus Pulse Diagram

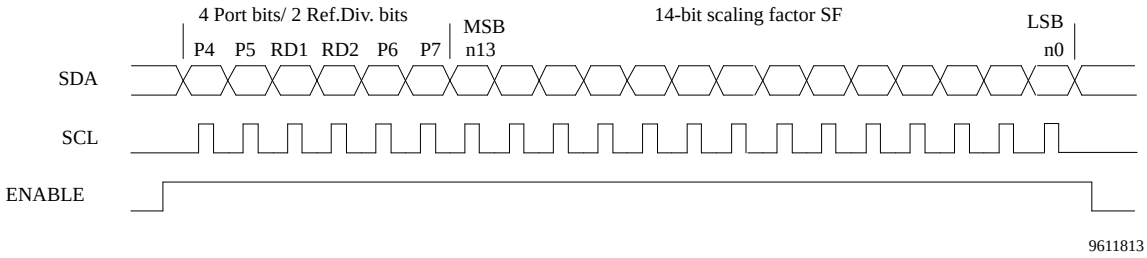


Figure 3.

n0 to n13	Scaling factor (SF)	SF = 8192 × n13 + 4096 × n12 + ... +2 × n1 + n0 SF - Range: 256..16383
P4 to P7	Port outputs	P4 - P7 = 1: port active
RD1, RD2	Reference divider selection	see table above

3-Wire Bus Timing

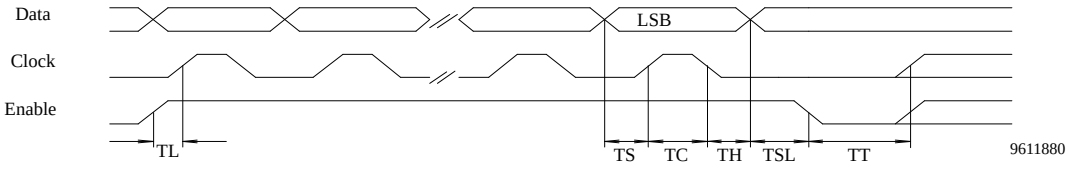
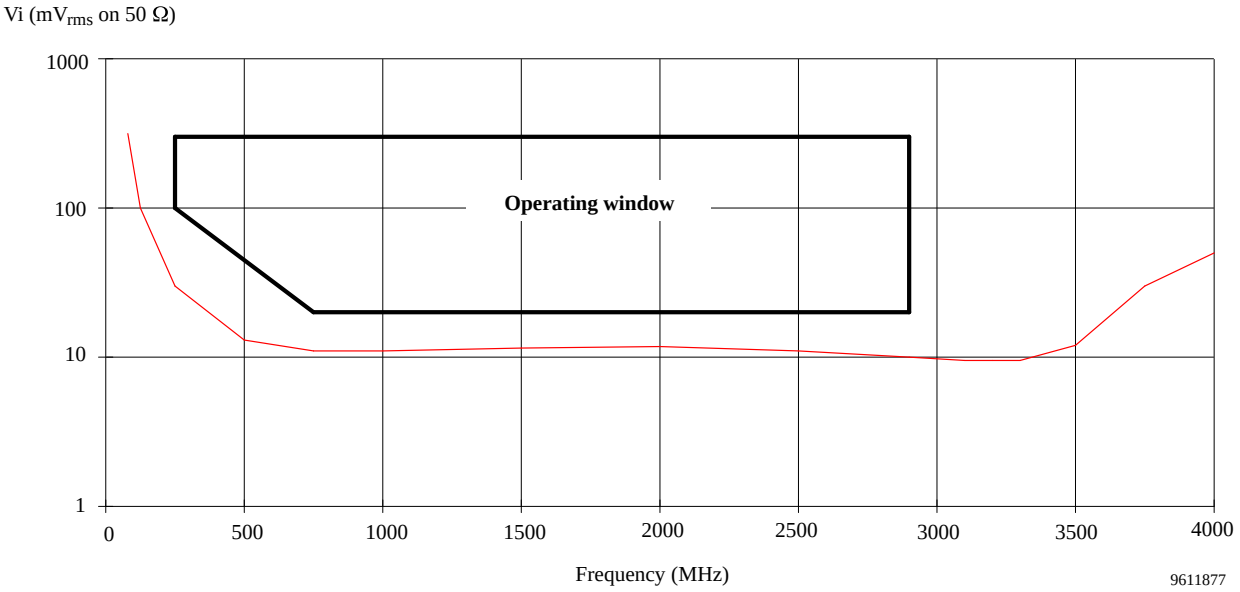


Figure 4.

Parameters	Symbol	Min.	Max.	Unit
Setup time	TS	2		µs
Enable hold time	TSL	2		µs
Clock width	TC	2		µs
Enable setup time	TL	10		µs
Enable between two transmissions	TT	10		µs
Data hold time	TH	2		µs

Typical Prescaler Input Sensitivity



Typical Input Impedence

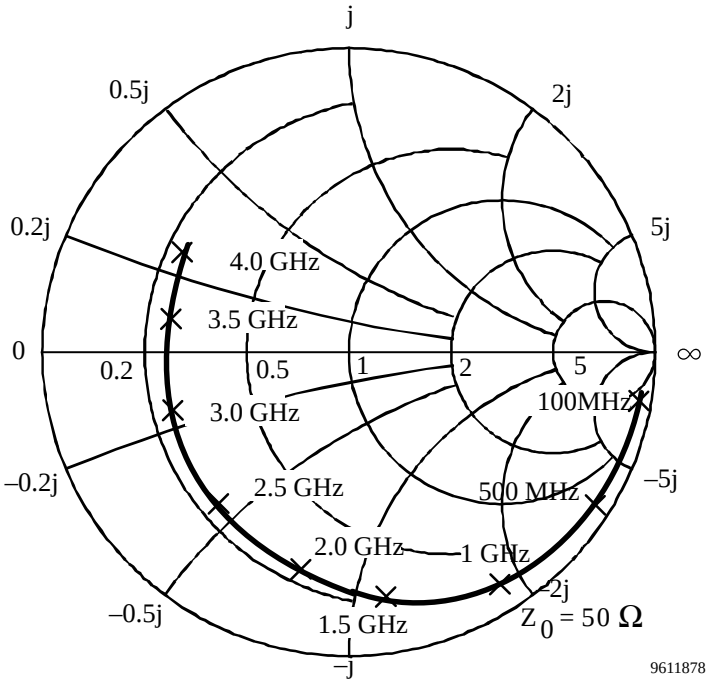


Figure 5.

Input/ Output Interface Circuits

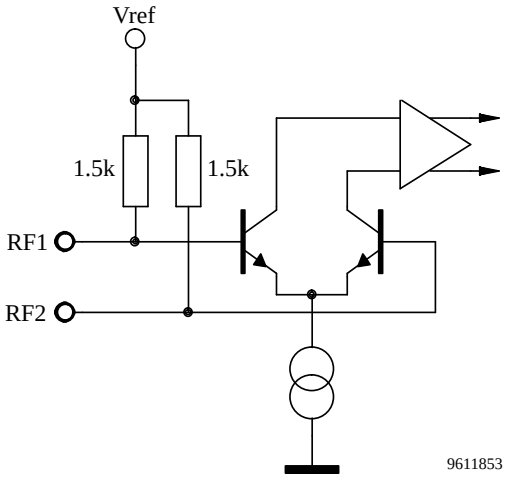


Figure 6. RF input

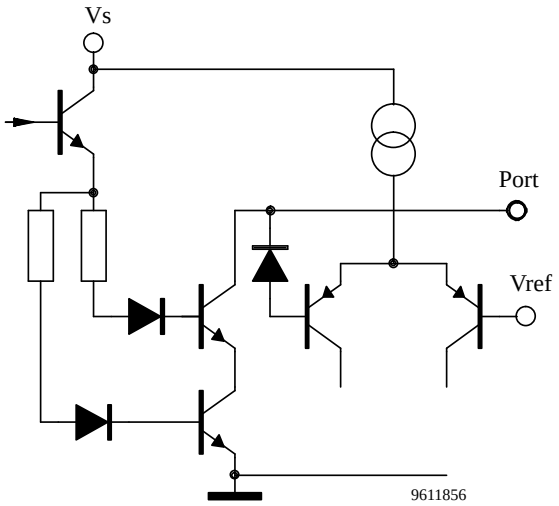


Figure 8. Ports P4, P5, P6, P7

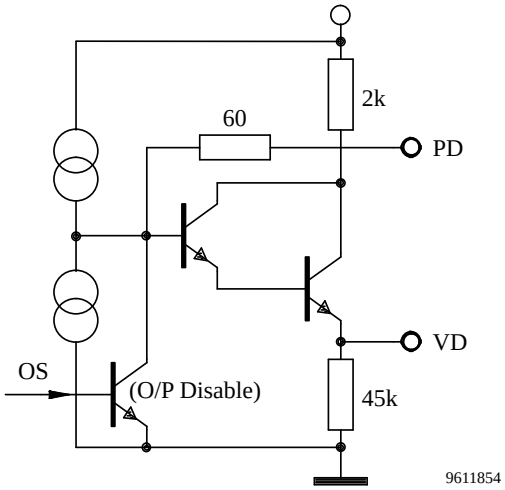


Figure 7. Loop amplifier

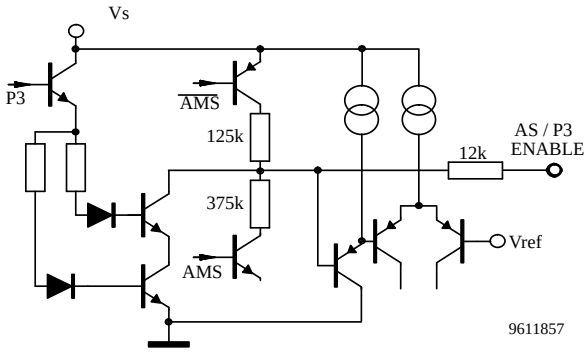


Figure 9. Address select/ Enable input/ Port output P3

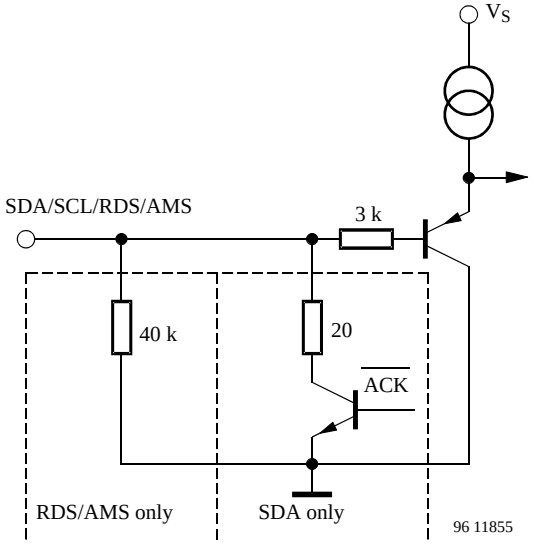


Figure 10. SCL/SDA and RDS/AMS input

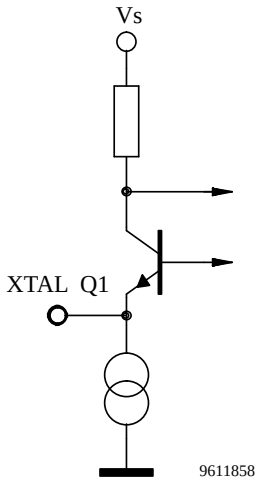


Figure 11. Reference oscillator

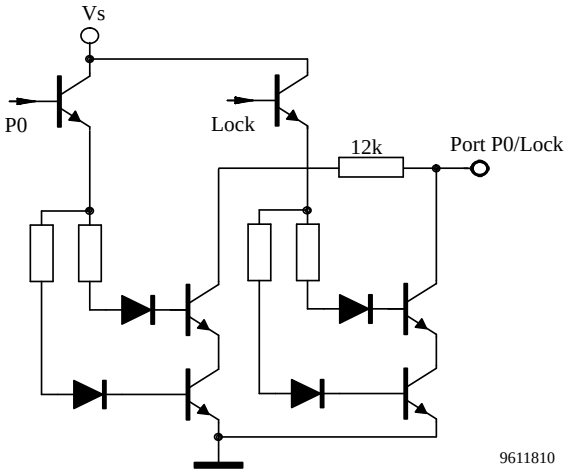


Figure 12. Port P0/ Lock output

Application Circuit

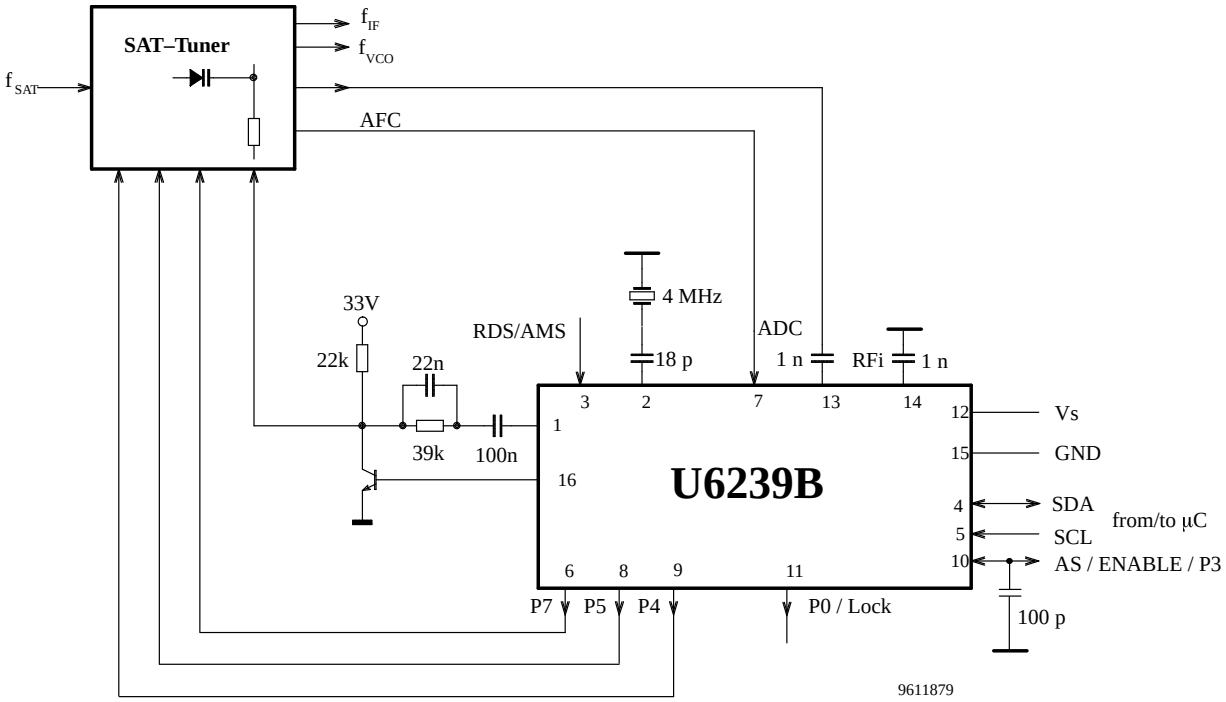
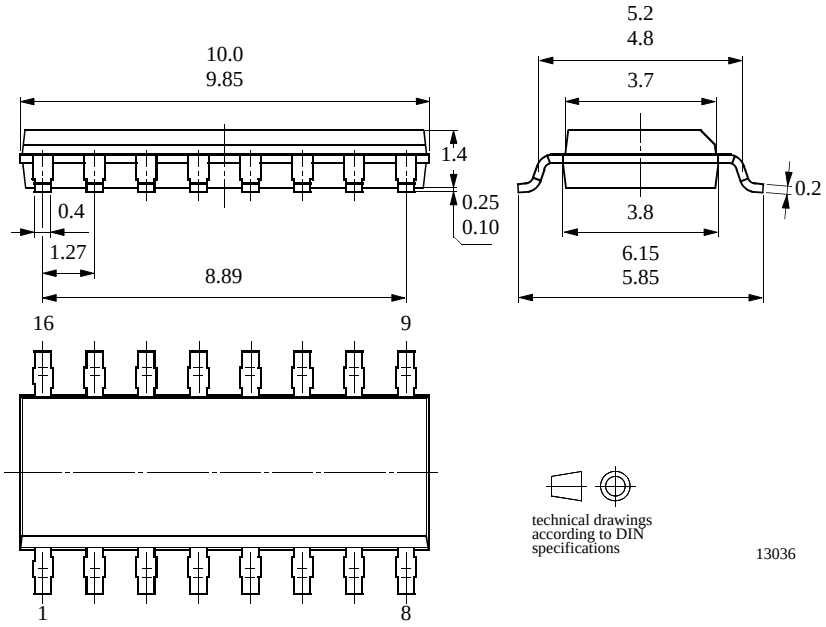


Figure 13.

Package Information

Package SO16
Dimensions in mm



Ozone Depleting Substances Policy Statement

It is the policy of **TEMIC TELEFUNKEN microelectronic GmbH** to

1. Meet all present and future national and international statutory requirements.

2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

TEMIC TELEFUNKEN microelectronic GmbH semiconductor division has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively

2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA

3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

TEMIC can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.

TEMIC TELEFUNKEN microelectronic GmbH, P.O.B. 3535, D-74025 Heilbronn, Germany
Telephone: 49 (0)7131 67 2831, Fax number: 49 (0)7131 67 2423