DISCONTINUED PRODUCT

NIPPON PRECISION CIRCUITS INC.

SM5128A1

CB Transceiver System LSI

OVERVIEW

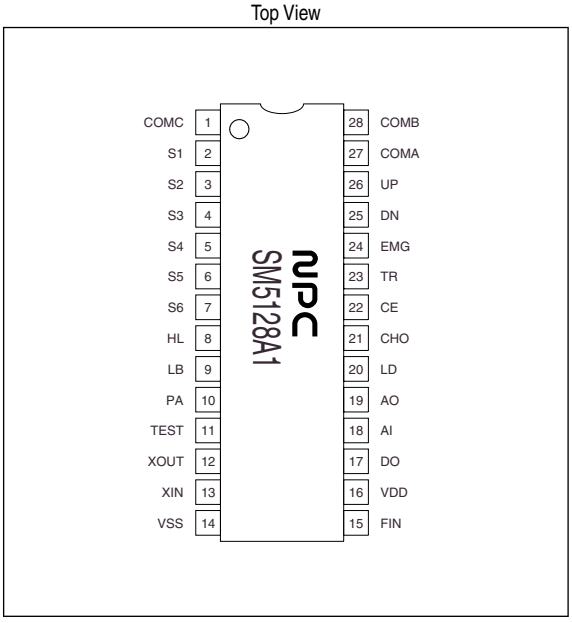
The SM5128A1 is a CB transceiver system CMOS IC that incorporates a PLL synthesizer, USA-frequency specification code ROM, channel up/down control circuit, LCD driver and channel-change unlock signal generator. All these features in a single chip allow the overall system cost to be reduced.

FEATURES

- USA-specification code ROM
- Channel up/down control circuit
- Unlock signal generator circuit
- Channel/PA display decoder
- LCD driver
- Channel-change confirmation tone output signal
- Amplifier for an active low-pass filter
- Single-crystal PLL synthesizer
- 4.5 to 5.5 V supply voltage
- 10.24 MHz crystal oscillator circuit
- 28-pin shrink DIP (SM5128A1N)
- 28-pin VSOP(SM5128A1V)
- Molybdenum-gate CMOS process

PINOUT

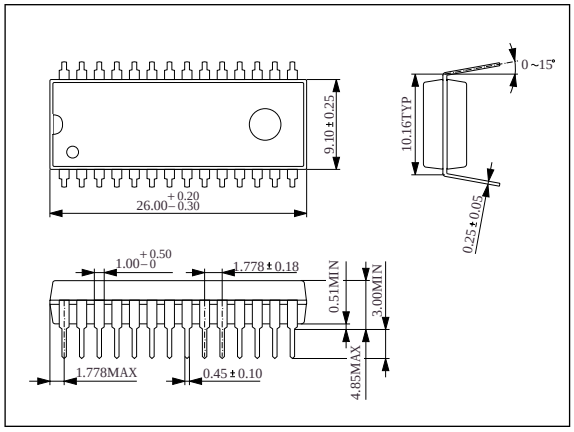
Top View



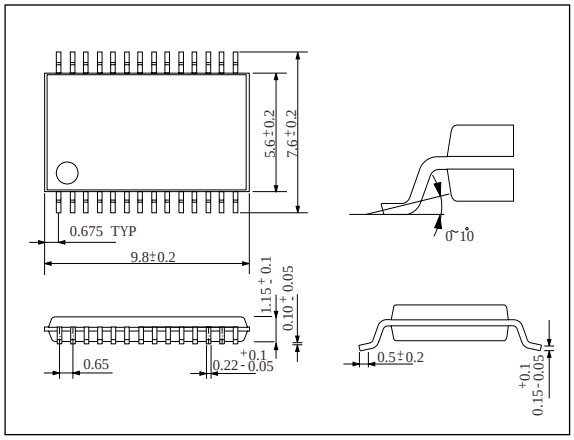
PACKAGE DIMENSIONS

Unit: mm

28-pin Shrink DIP



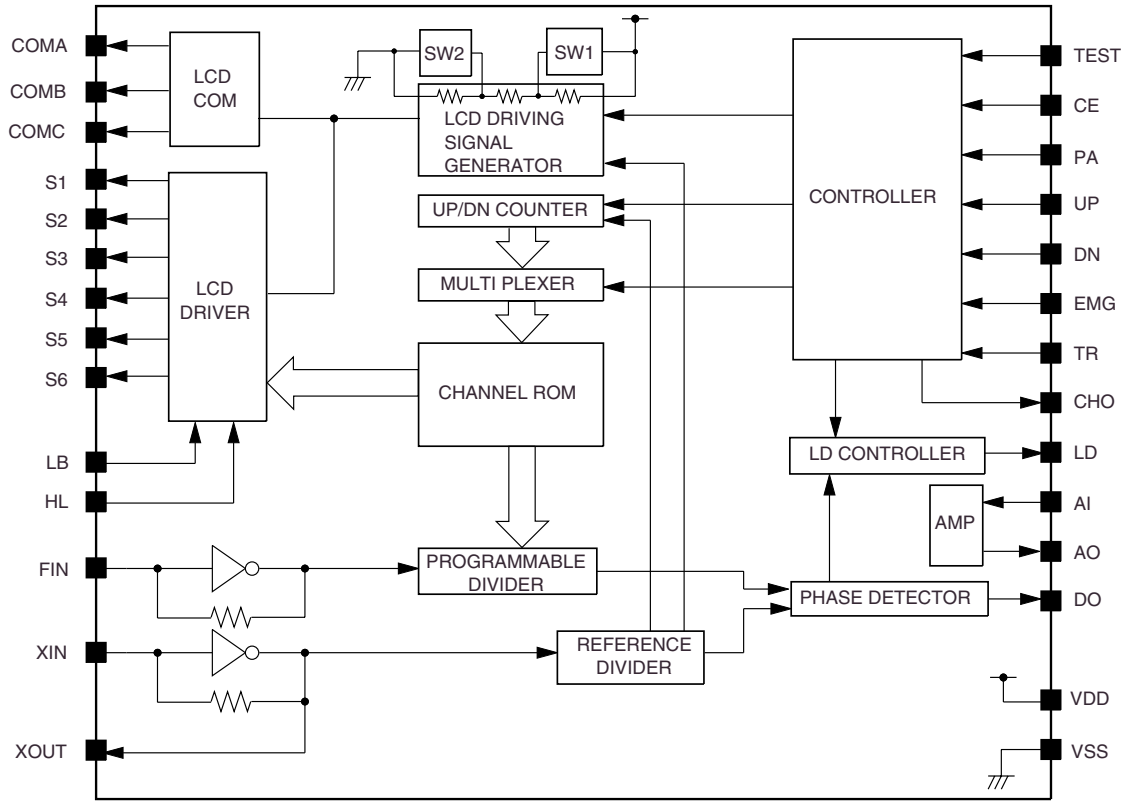
28-pin VSOP



ORDERING INFOMATION

Device	Package
SM5128A1N	28pin SDIP
SM5128A1V	28pin VSOP

BLOCK DIAGRAM



PIN DESCRIPTION

Number	Name	Description
1	COMC	LCD common drive signal output
2 to 7	S1 to S6	LCD segment drive signal output
8	HL	“HIGH POWER”/”LOW POWER” display indicator control input. “HIGH POWER” indicator when HIGH, and “LOW POWER” indicator when LOW or open. Pull-down resistor built-in.
9	LB	“LOW BATTERY” display indicator input. “LOW BATTERY” indicator when LOW or open. Pull-down resistor built-in.
10	PA	PA input. PA mode when HIGH. Pull-down resistor built-in.
11	TEST	Test input. Tie LOW or open for normal operation.
12	XOUT	Crystal oscillator circuit input and output
13	XIN	
14	VSS	Ground
15	FIN	Programmable counter input. Feedback resistor built-in.
16	VDD	4.5 to 5.5 V supply voltage
17	DO	Phase detector output. Three-state output pin.
18	AI	Inverter input and output. AI is HIGH in standby mode.
19	AO	
20	LD	Unlock signal output. Unlocked when LOW, and locked when HIGH.
21	CHO	Channel-change confirmation tone output. Active-HIGH pulse of approximately 50 ms duration.

Number	Name	Description
22	CE	PLL start pin. Start when HIGH, and standby mode when LOW. Pull-down resistor built-in.
23	TR	Transmit/Receive switch input. Transmit when HIGH, and receive when LOW or open. Pull-down resistor built-in.
24	EMG	Emergency channel select input. Channel 9 when HIGH, and the previously set channel with channel up/down control when LOW or open. Pull-down resistor built-in.
25	UP	Channel-change up control input. Change up when HIGH. Pull-down resistor built-in.
26	DN	Channel-change down control input. Change down when HIGH. Pull-down resistor built-in.
27	COMA	LCD common drive signal outputs
28	COMB	

SPECIFICATIONS

Absolute Maximum Ratings

V_{SS} = 0 V

Parameter	Symbol	Condition	Rating	Unit
Supply voltage	V_{DD}		–0.3 to 7.0	V
Input voltage range	V_{IN}		V_{SS} to V_{DD}	V
Power dissipation	P_D		150	mW
Operating temperature	T_{opr}		–30 to 80	°C
Storage temperature range	T_{stg}		–40 to 125	°C
Soldering temperature	T_{sld}		255	°C
Soldering time	t_{sld}		10	s
Output current	I_O		10	mA

Recommended Operating Conditions

V_{SS} = 0 V

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Supply voltage	V_{DD}		4.5	5.0	5.5	V

Electrical Characteristics

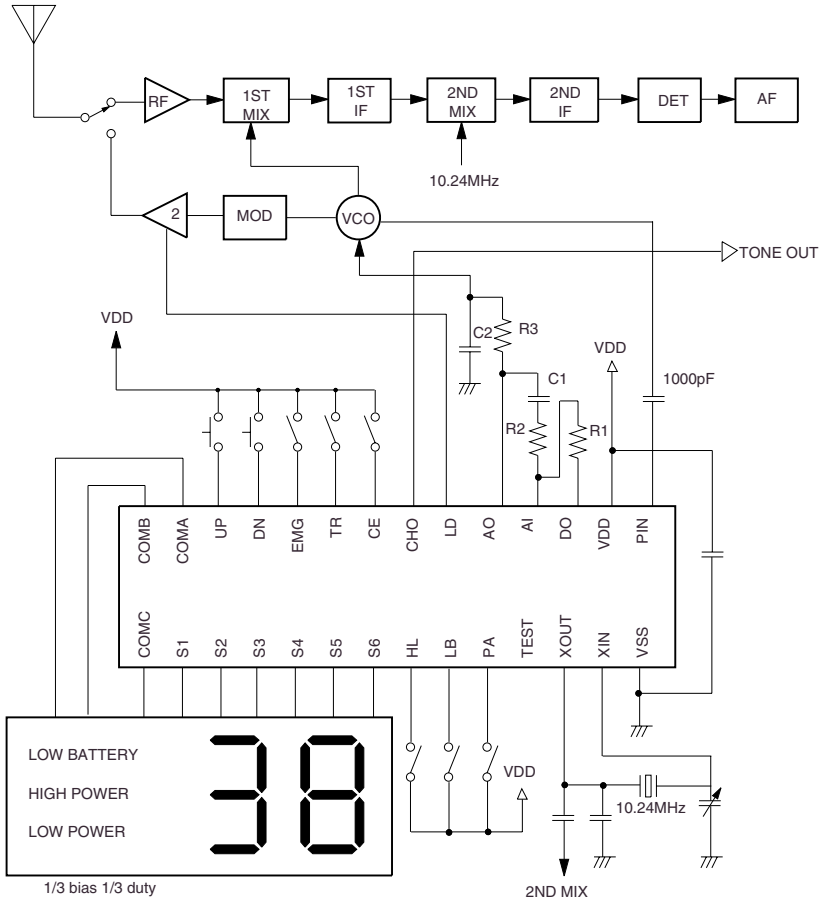
V_{SS} = 0 V, Ta=–30 to 80 ˚C, V_{DD}=4.5 to 5.5V unless otherwise noted

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Operating consumption current[1]	I_{DD}		–	–	10	mA
FIN maximum operating frequency	f_{max1}	1.0 Vp-p sine wave	18	–	–	MHz
XIN maximum operating frequency	f_{max2}	1.0 Vp-p sine wave	12	–	–	MHz
FIN operating input voltage	V_{IN1}	18 MHz sine wave	1.0	–	V_{DD} – 1	Vp-p
XIN operating input voltage	V_{IN2}	10.24 MHz sine wave	1.0	–	V_{DD} – 1	Vp-p
LOW-level input voltage[2]	V_{IL1}		–	–	0.4	V
HIGH-level input voltage[2]	V_{IH1}		V_{DD} – 0.4	–	–	V
FIN and XIN start voltage	V_{IO}	V_{DD} = 5.0 V	2.0	2.5	3.0	V

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
FIN and XIN LOW-level input current	I_{IL1}	V_{IL1} = 0 V, V_{DD} = 5.5 V	–	–	20	µA
FIN and XIN HIGH-level input current	I_{IH1}	V_{IH1} = V_{DD}, V_{DD} = 5.5 V	–	–	20	µA
LOW-level input current[2]	I_{IL2}	V_{IL2} = 0 V, V_{DD} = 5.5 V	–	–	1	µA
HIGH-level input current[2]	I_{IH2}	V_{IH2} = V_{DD}, V_{DD} = 5.5 V	–	100	200	µA
AI LOW-level input current	I_{IL3}	V_{IL3} = 0 V, V_{DD} = 5.5 V, T_a = 25 °C	–	0.001	1	µA
AI HIGH-level input current	I_{IH3}	V_{IH3} = V_{DD}, V_{DD} = 5.5 V, T_a = 25 °C	–	0.001	1	µA
Standby current	I_{STB}	CE = open, T_a = 25 °C	–	0.001	1	µA
COMA, COMB, COMC LOW-level output voltage	V_{OL1}	I_{OL} = 10 µA	–	–	0.4	V
COMA, COMB, COMC HIGH-level output voltage	V_{OH1}	I_{OH} = 10 µA	V_{DD} – 0.4	–	–	V
S1 to S6 LOW-level output voltage	V_{OL2}	I_{OL} = 10 µA	–	–	0.4	V
S1 to S6 HIGH-level output voltage	V_{OH2}	I_{OH} = 10 µA	V_{DD} – 0.4	–	–	V
LD, CHO, DO LOW-level output voltage	V_{OL3}	I_{OL} = 0.4 mA	–	–	0.4	V
LD, CHO, DO HIGH-level output voltage	V_{OH3}	I_{OH} = 0.4 mA	V_{DD} – 0.4	–	–	V
AO LOW-level output voltage	V_{OL4}	I_{OL} = 0.4 mA, AI = V_{DD}	–	–	0.4	V
AO HIGH-level output voltage	V_{OH4}	I_{OH} = 0.4 mA, AI = 0 V	V_{DD} – 0.4	–	–	V
XOUT LOW-level output voltage	V_{OL5}	I_{OL} = 0.1 mA, XIN = V_{DD}	–	–	0.4	V
XOUT HIGH-level output voltage	V_{OH5}	I_{OH} = 0.1 mA, XIN = 0 V	V_{DD} – 0.4	–	–	V
DO, AI HIGH-level leakage current	I_{LH}	V_{IH4} = V_{DD}, V_{DD} = 5.5 V, T_a = 25 °C	–	–	100	nA
DO, AI LOW-level leakage current	I_{LL}	V_{IL4} = 0 V, V_{DD} = 5.5 V, T_a = 25 °C	–	–	100	nA

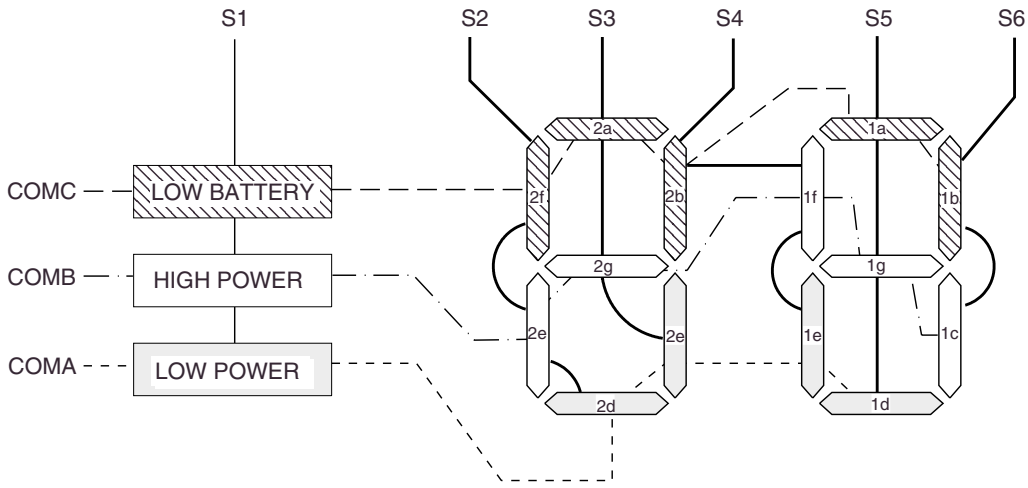
1. FIN = 16.71 MHz and 1.0 Vp-p, XIN = 10.24 MHz and 1.0 Vp-p
2. Pins HL, LB, PA, TEST, CE, TR, EMG, DN, UP.

TYPICAL APPLICATION



Display Font

LCD Segment Diagram

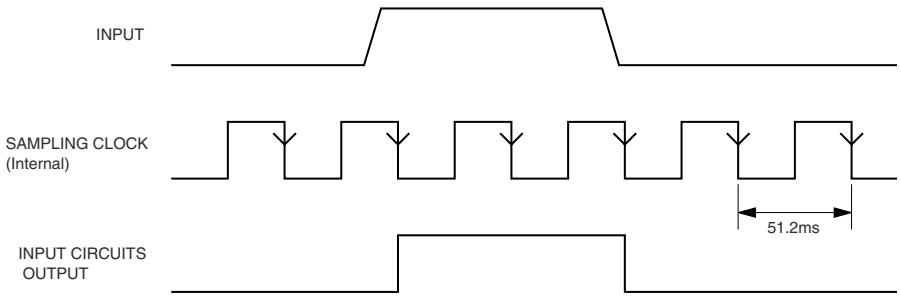


Common	S1	S2	S3	S4	S5	S6
COMA	LOW POWER	2d	2c	1e	1d	–
COMB	HIGH POWER	2e	2g	1f	1g	1c
COMC	LOW BATTERY	2f	2a	2b	1a	1b

FUNCTIONAL DESCRIPTION

Input Timing

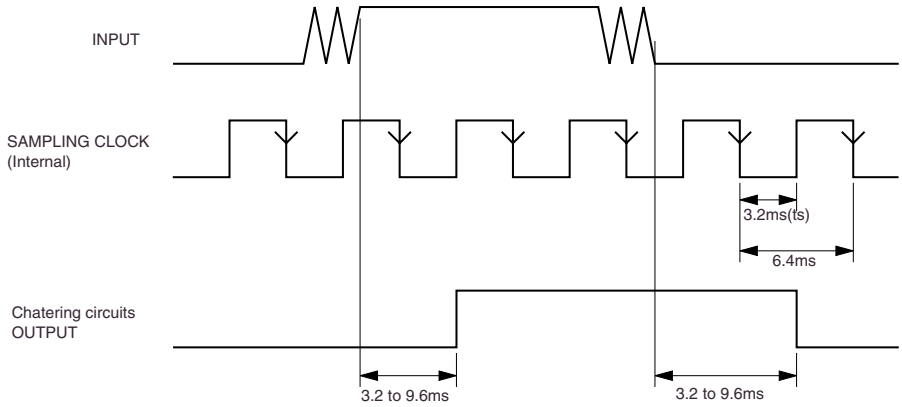
The input timing for pins HL, LB, PA, TR and EMG is shown in the following figure.



Note that data is read in on the falling edge of the sampling clock.

Chattering Elimination Circuit

A high-speed chattering elimination circuit is incorporated in pins UP and DN. The chattering elimination circuit recognizes the input state only after the input has been continuously LOW or HIGH for a period of 3.2 to 6.4 ms. The output does not change if the input state lasts less than 3.2 ms.



Note that the input is recognized during the LOW-level pulse interval, t_S (32 ms), of the sampling clock.

CE

CE is the chip enable pin. Normal operation is selected when CE is HIGH, and standby mode is selected when CE is LOW. CE incorporates a pull-down resistor.

In standby mode, the following states occur.

- All pins except CE are ignored.
- Crystal oscillator is stopped. XIN is HIGH, and XOUT is LOW.
- PLL operation is stopped. DO and LD are high impedance, AI and FIN are HIGH, and AO and CHO are LOW.
- Display segments are all OFF. COMA, COMB, COMC, and S1 to S6 are LOW.
- Current channel selection is stored.

PA

PA is the PA display mode select pin. PA mode is selected when pin PA is HIGH. When PA is open, PLL operation is restored. PA incorporates a pull-down resistor.

In PA display mode, PLL operation is stopped and the following states occur.

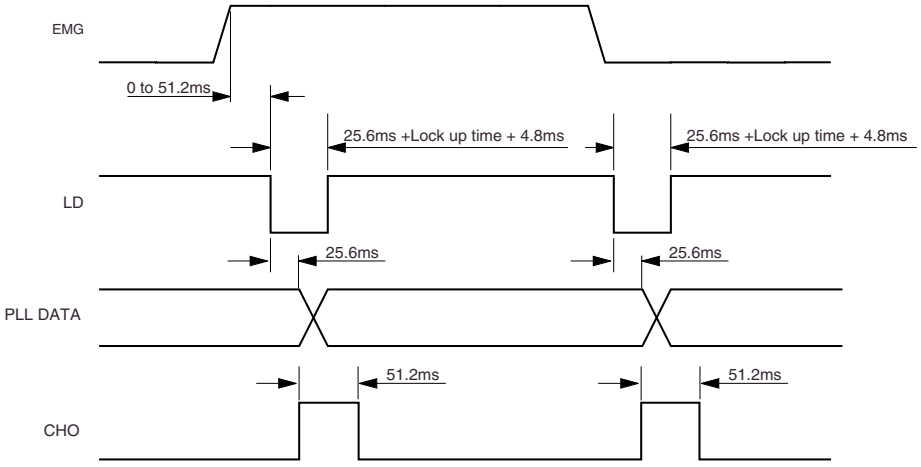
- FIN and AI are HIGH.
- CHO is LOW.
- DO and LD are high impedance.
- Current channel selection is stored.
- “HIGH POWER” and “LOW POWER” display indicators are OFF.

TR

TR is the transmit/receive select pin. Transmit is selected when TR is HIGH, and receive is selected when TR is LOW or open. When transmit mode is selected, the channel up/down control is disabled, and the state of pin EMG is accepted. TR incorporates a pull-down resistor.

EMG

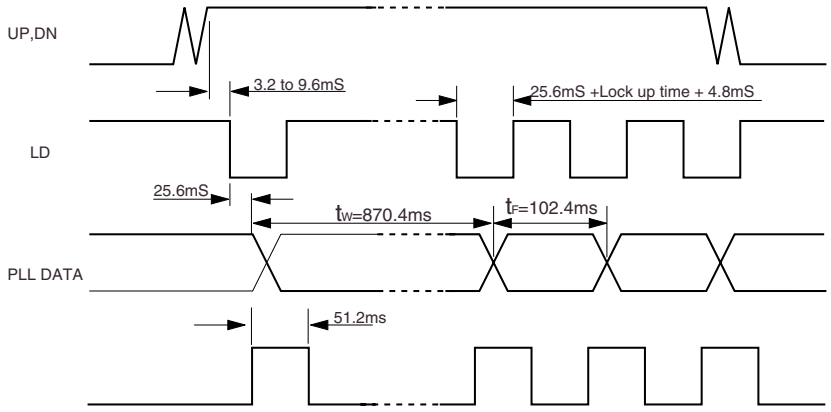
EMG is the emergency channel select pin. The emergency channel, channel 9, is selected when EMG is HIGH, and the previously selected channel, determined by the state of pins UP and DN, is selected when EMG is LOW or open. EMG incorporates a pull-down resistor.



UP and DN

UP and DN are the channel up/down control pins, respectively. They also serve as the fast up/down function controls, in addition to their step up/down functions. The fast change function is selected and the channel change cycle becomes faster when a key corresponding to either input pin is pressed continuously for a period longer than the wait time t_W.

Channel up/down operation is selected when EMG and PA are LOW. Up/down operation is disabled when CE is LOW (standby mode) and when TR is HIGH (transmit mode).

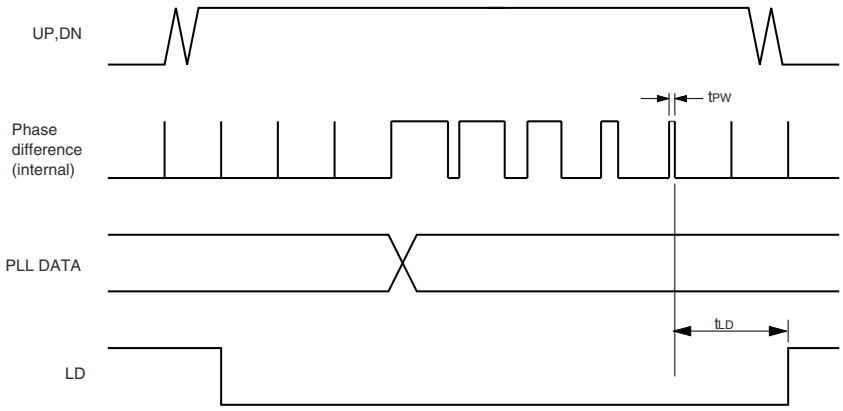


LD

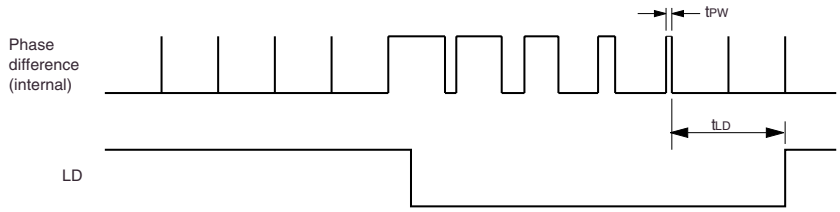
LD is the unlock detector pin. The PLL is locked when LD is HIGH, and the PLL is unlocked when LD is LOW.

LD goes LOW when UP, DN, TR and EMG are LOW (case 1), and when the PLL becomes unlocked due to an external disturbance (case 2).

Inputs are LOW (case 1)



External disturbance (case 2)



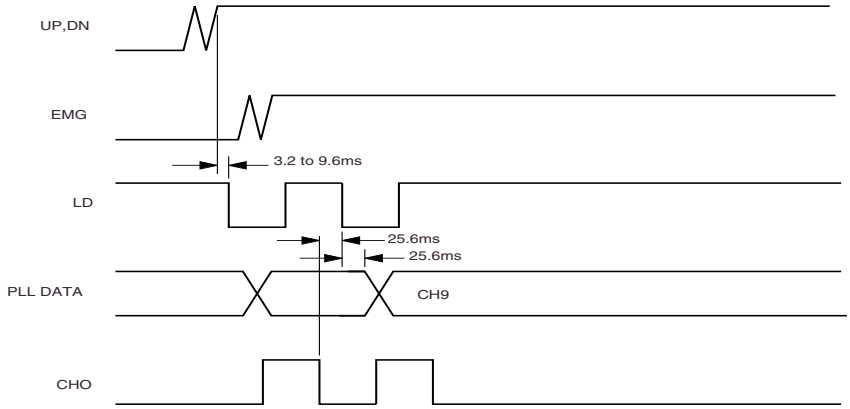
When the internal phase difference t_{PW} exceeds 1.6 µs, the PLL unlocks and LD goes LOW. Subsequently, when the difference is less than 1.6 µs for a period of 4.8 ms, the hPLL locks and LD goes HIGH.

Input Pin Priority

The device operation for all possible input combinations is determined by the active level of the inputs using the following input pin priority.

CE > PA > EMG > UP > DN

If a high priority pin goes LOW (active) while a lower priority pin operation is in progress (from when LD goes LOW until CHO output stops), the operation stops and the higher priority pin operation takes precedence.



CHO

CHO is the channel change confirmation tone output, and indicates that the frequency changed due to switching UP, DN, TR and EMG. The output signal is a 2.5 kHz tone of approximately 51.2 ms duration.

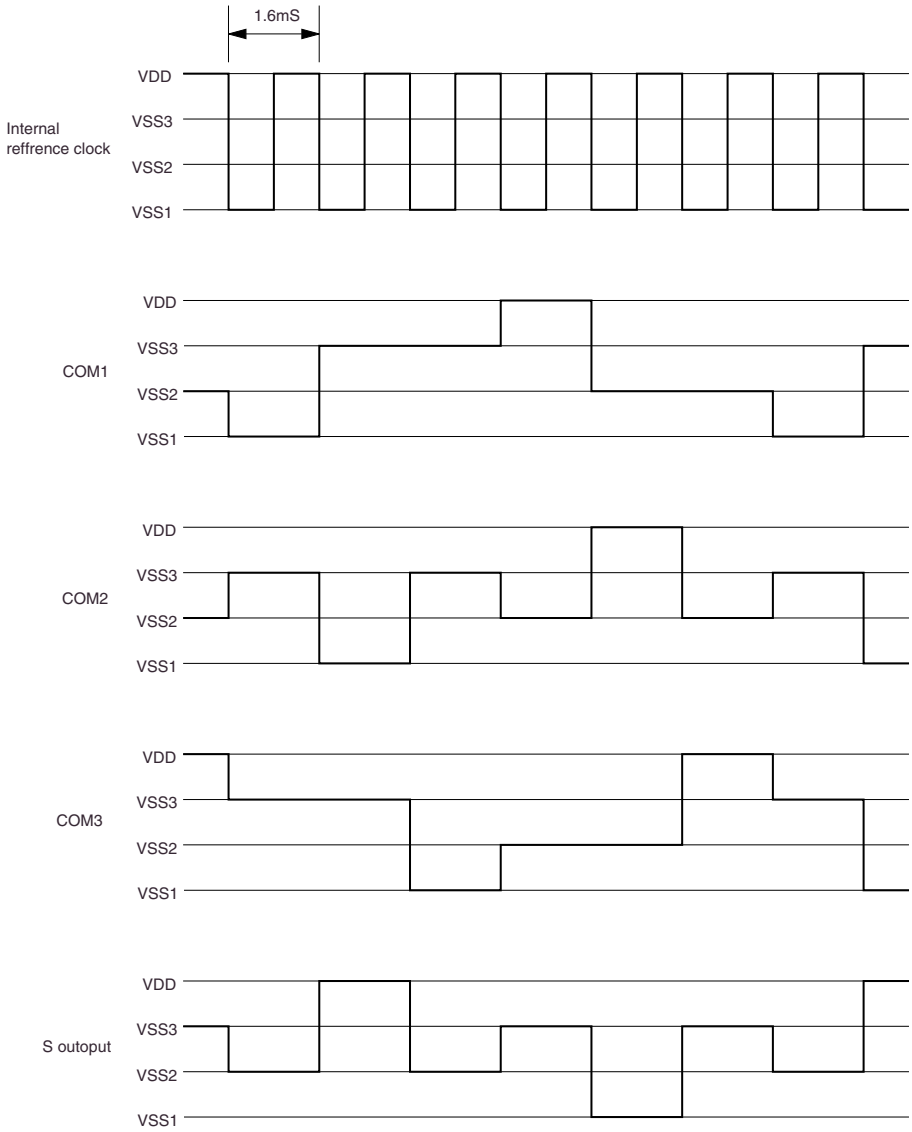
LB

LB is the “LOW BATTERY” display indicator control input. The indicator is lit when LB is LOW or open, and the indicator is OFF when LB is HIGH. LB incorporates a pull-down resistor. The state of LB does not affect PLL operation.

HL

HL is the “HIGH POWER” and “LOW POWER” display indicators control input. The “HIGH POWER” indicator is lit when HL is HIGH, and the “LOW POWER” indicator is lit when HL is LOW or open. HL incorporates a pull-down resistor. The state of HL does not affect PLL operation.

LCD Common/Segment Output Waveforms



Power-ON Initialization

When power is applied between VDD and VSS, the channel up/down and other controls are disabled in the current channel is channel 9.

FREQUENCY TABLE

USA-speciÞcation

Channel	TR = HIGH		TR = LOW (open)	
	N (T)	VCO (MHz)	N (R)	VCO (MHz)
1	5393	13.4825	3254	16.27
2	5395	13.4875	3256	16.28
3	5397	13.4925	3258	16.29
4	5401	13.5025	3262	16.31
5	5403	13.5075	3264	16.32
6	5405	13.5125	3266	16.33
7	5407	13.5175	3268	16.34
8	5411	13.5275	3272	16.36
9	5413	13.5325	3274	16.37
10	5415	13.5375	3276	16.38
11	5417	13.5425	3278	16.39
12	5421	13.5525	3282	16.41
13	5423	13.5575	3284	16.42
14	5425	13.5625	3286	16.43
15	5427	13.5675	3288	16.44
16	5431	13.5775	3292	16.46
17	5433	13.5825	3294	16.47
18	5435	13.5875	3296	16.48
19	5437	13.5925	3298	16.49
20	5441	13.6025	3302	16.51
21	5443	13.6075	3304	16.52
22	5445	13.6125	3306	16.53
23	5451	13.6275	3312	16.56
24	5447	13.6175	3308	16.54
25	5449	13.6225	3310	16.55
26	5453	13.6325	3314	16.57
27	5455	13.6375	3316	16.58
28	5457	13.6425	3318	16.59
29	5459	13.6475	3320	16.60
30	5461	13.6525	3322	16.61
31	5463	13.6575	3324	16.62
32	5465	13.6625	3326	16.63
33	5467	13.6675	3328	16.64
34	5469	13.6725	3330	16.65
35	5471	13.6775	3332	16.66
36	5473	13.6825	3334	16.67
37	5475	13.6875	3336	16.68
38	5477	13.6925	3338	16.69

Channel	TR = HIGH		TR = LOW (open)	
	N (T)	VCO (MHz)	N (R)	VCO (MHz)
39	5479	13.6975	3340	16.70
40	5481	13.7025	3342	16.71

DISCONTINUED PRODUCT

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NC9608BE 2001.06