

***THIS DOCUMENT IS FOR MAINTENANCE  
PURPOSES ONLY AND IS NOT  
RECOMMENDED FOR NEW DESIGNS***

# NJ88C30

## VHF SYNTHESISER

The NJ88C30 contains all the logic needed for a VHF PLL synthesiser and is fabricated on the GPS high performance, small geometry CMOS process. The circuit contains a reference oscillator and divider, a two-modulus prescaler and 4-bit control register, a 12-bit programmable divider, a phase comparator and the necessary data input and control logic.

### FEATURES

- Low Power CMOS
- Easy to Use
- Low Cost
- Single Chip Synthesiser to VHF
- Lock Detect Output

### APPLICATIONS

- Mobile Radios
- Hand Held Portable Radios
- Sonobuoys

### ORDERING INFORMATION

- NJ88C30 KA DP** Plastic DIL Package
- NJ88C30 KA MP** Miniature Plastic DIL Package

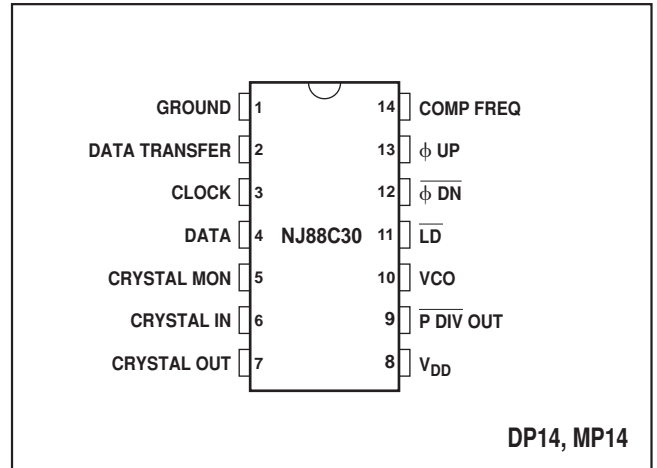


Fig.1 Pin connections - top view

### ABSOLUTE MAXIMUM RATINGS

Supply voltage, $V_{DD}$	-0.3V to 6V
Voltage on any pin	-0.3V to $V_{DD} + 0.3V$
Operating temperature	-30°C to +70°C
Storage temperature	-55°C to +125°C

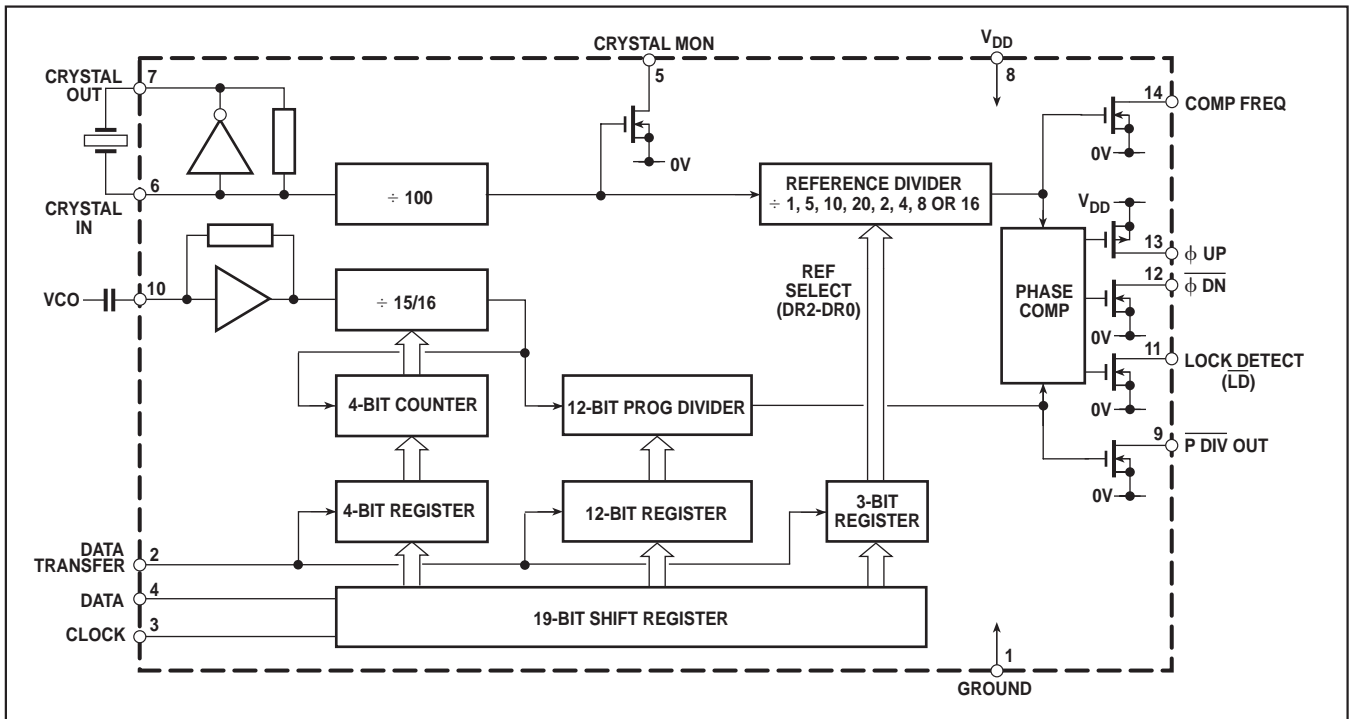


Fig.2 Block diagram

# NJ88C30

## ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

$$T_{AMB} = -30^{\circ}\text{C to } +70^{\circ}\text{C}, V_{DD} = 5\text{V} \pm 0.5\text{V}$$

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	8		4	7	mA	1VRMS VCO input at 200MHz and $f_{XTAL} = 10\text{MHz}$
<b>Crystal Oscillator</b>						
Frequency	6, 7		10	15	MHz	Parallel resonant, fundamental crystal
External input level	6	1			Vrms	AC coupled
High level	6	$V_{DD}-1$			V	DC coupled
Low level	6			1	V	DC coupled
<b>VCO Input</b>						
Input sensitivity	10	1			Vrms	At 200MHz, see Fig. 3
Slew rate	10	4			V/ $\mu\text{s}$	
Input impedance	10		5pF// 10k			
<b>DATA, DATA TRANSFER and CLOCK Inputs</b>						
High level	2, 3, 4	$V_{DD}-1$			V	See Fig. 4
Low level	2, 3, 4			1	V	
Rise, fall time	2, 3			200	ns	
Data set-up time	3, 4	200			ns	
Clock frequency	3			2	MHz	
Transfer pulse width	2	500			ns	
<b>CRYSTAL MONITOR Output</b>						
Current sink	5	0.8			mA	$V_{OUT} = 0.5\text{V}$
<b>COMP FREQ, LD, P DIV</b>						
Current sink	9, 11, 14	1.6			mA	$V_{OUT} = 0.5\text{V}$
$\phi$ UP / $\phi$ DN						
Current sink	12	0.8			mA	$V_{OUT} = 0.5\text{V}$
Current source	13	0.8			mA	$V_{OUT} = V_{DD}-0.5\text{V}$

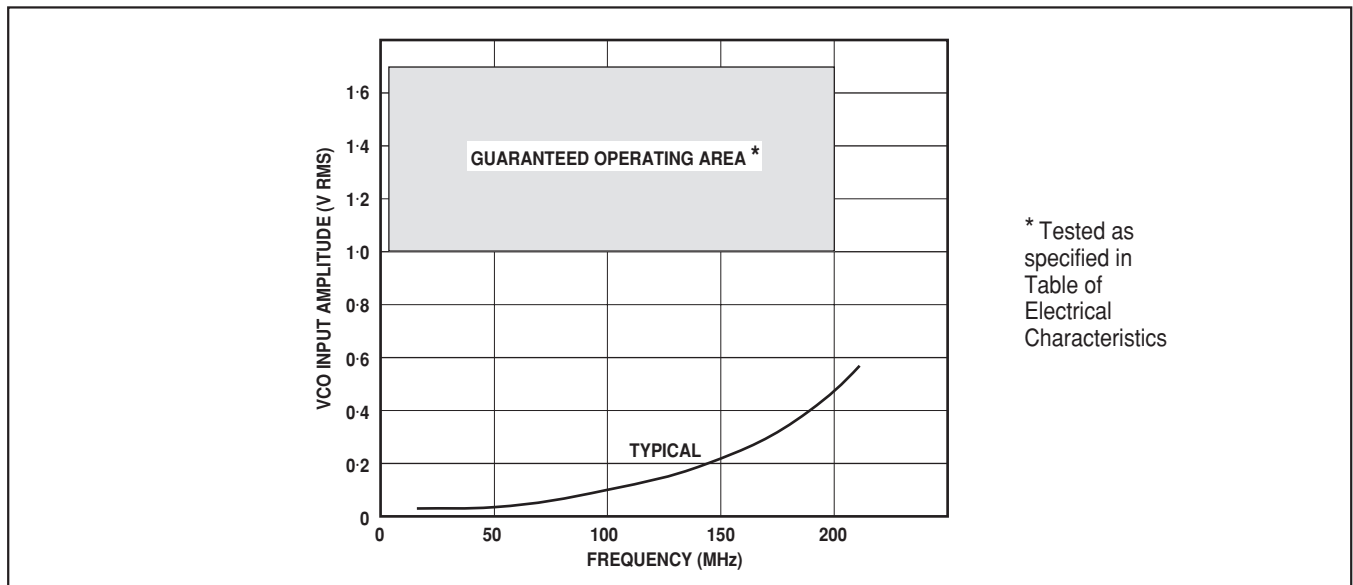


Fig. 3 Input sensitivity

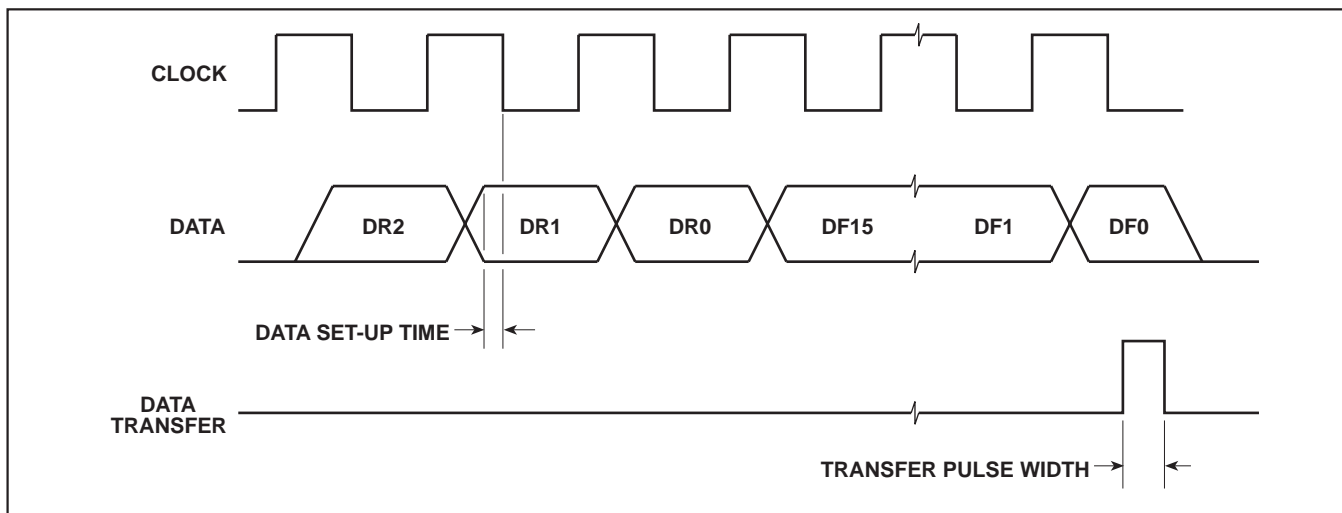


Fig. 4 Input data timing diagram

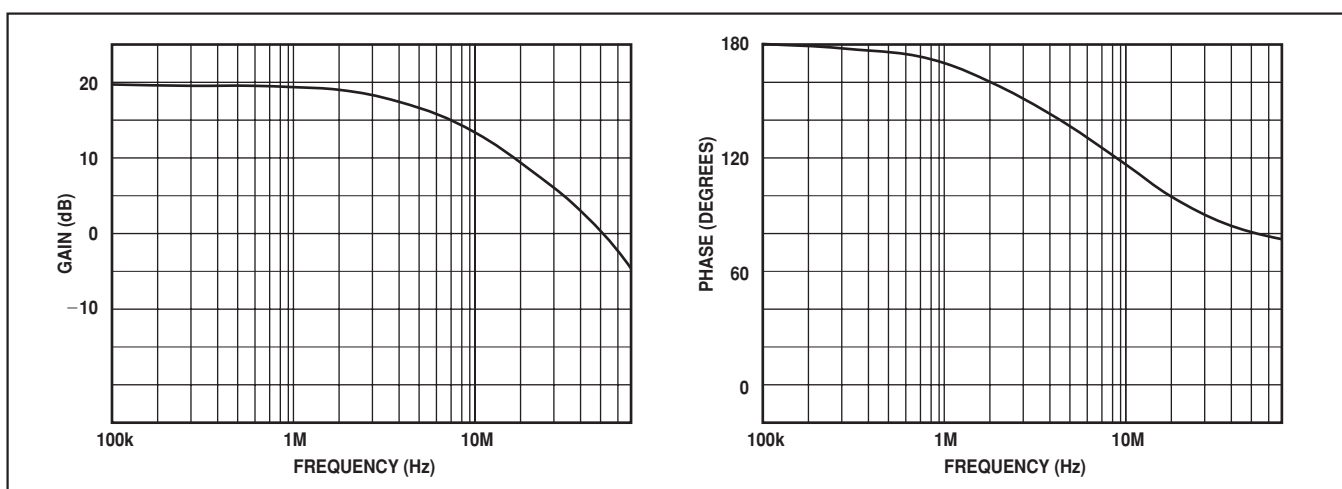


Fig. 5 Gain and phase characteristics of reference oscillator inverter

**CIRCUIT DESCRIPTION**

**Crystal Oscillator and Reference Divider**

The Reference oscillator consists of a Pierce type oscillator intended for use with a parallel resonant fundamental crystal. Typical gain and phase characteristics for the oscillator inverter are shown in Fig 5. An external reference oscillator may be used by either capacitively coupling a 1V RMS sinewave into CRYSTAL IN (pin 6) or, if CMOS levels are available, by direct connection to CRYSTAL IN.

The reference oscillator drives a ÷100 prescaler followed by a reference divider to provide a range of comparison frequencies which are selected by decoding the first three bits (DR2, DR1, DR0) of the input data. The possible division ratios and the comparison frequencies (channel spacing) if a 10MHz crystal is used are shown in Table 1.

DR2	DR1	DR0	Total division ratio	Comparison frequency for 10MHz Ref. Osc.
0	0	0	1600	6.25kHz
0	0	1	800	12.5kHz
0	1	0	400	25kHz
0	1	1	200	50kHz
1	0	0	2000	5kHz
1	0	1	1000	10kHz
1	1	0	500	20kHz
1	1	1	100	100kHz

Table 1 Reference divider division ratios

To assist in trimming the crystal, an open drain output at one hundredth of the reference oscillator frequency is provided on CRYSTAL MONITOR pin 5

**Programmable Divider**

The programmable divider consists of a ÷15/16 two modulus prescaler with a 4-bit control register, followed by a 12-bit programmable divider. A 1V RMS sinewave should be capacitively coupled from the VCO to the divider input VCO pin (pin 10).

The overall division ratio is selected by a single 16-bit word (DF15 to DF0), loaded through the serial data bus. A lower limit of 240 ensures correct prescaler operation; the upper limit is 65535. The VCO frequency in a locked system will be this division ratio multiplied by the comparison frequency.

**Phase Comparator**

The phase comparator consists of a digital type phase comparator with open drain  $\phi$  UP and  $\phi$  DN outputs and an open drain LOCK DETECT (LD) output. Open drain outputs from the reference divider and programmable divider are provided for monitoring purposes or for use with an external phase comparator. Waveforms for all these outputs are shown in Fig.6. The duty cycle of  $\phi$  UP and  $\phi$  DN versus phase difference are shown in Fig. 7. The phase comparator is linear over a  $\pm 2\pi$  range and if the phase gains or slips by more than  $2\pi$ , the phase comparator outputs repeat with a  $2\pi$  period.

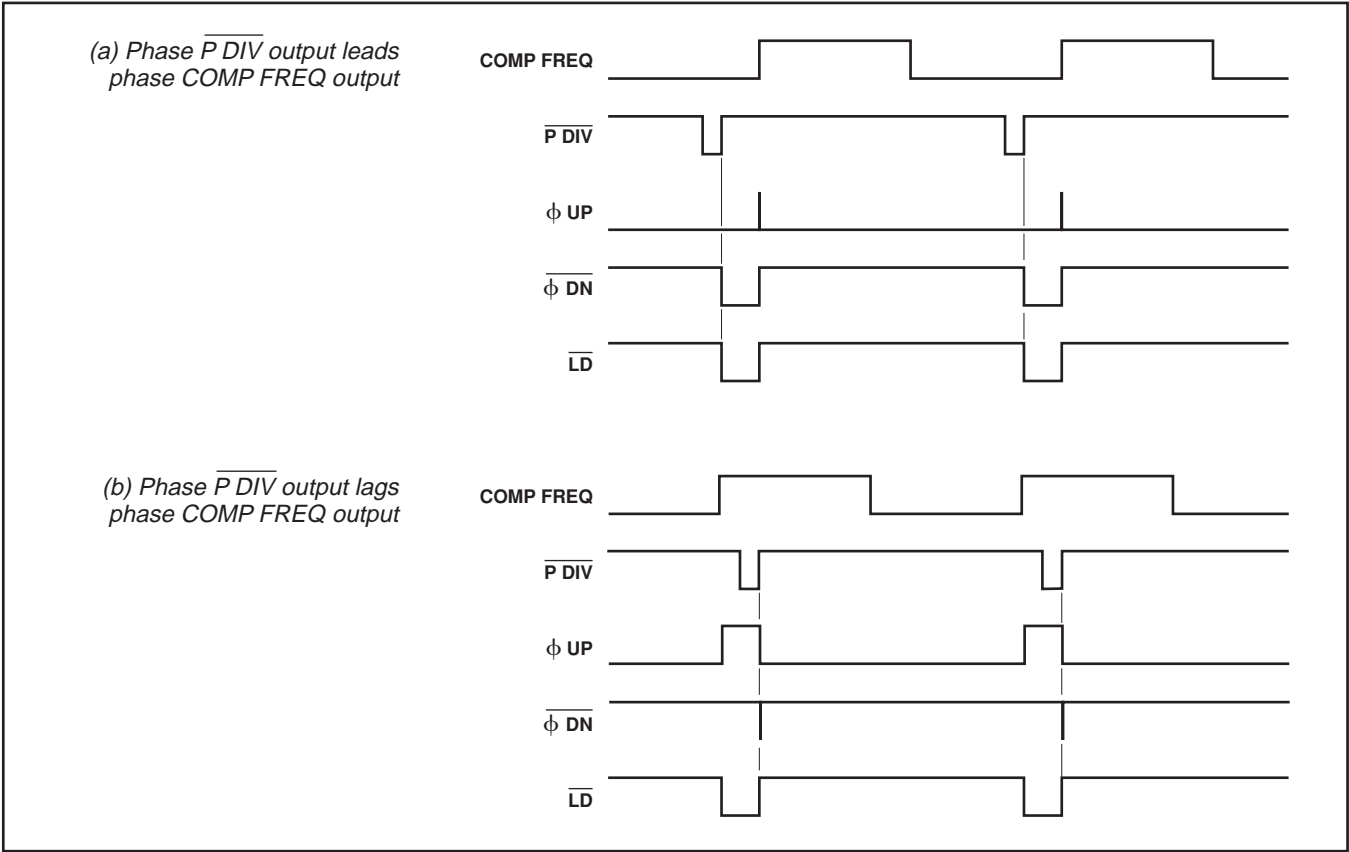


Fig. 6 Phase comparator waveforms

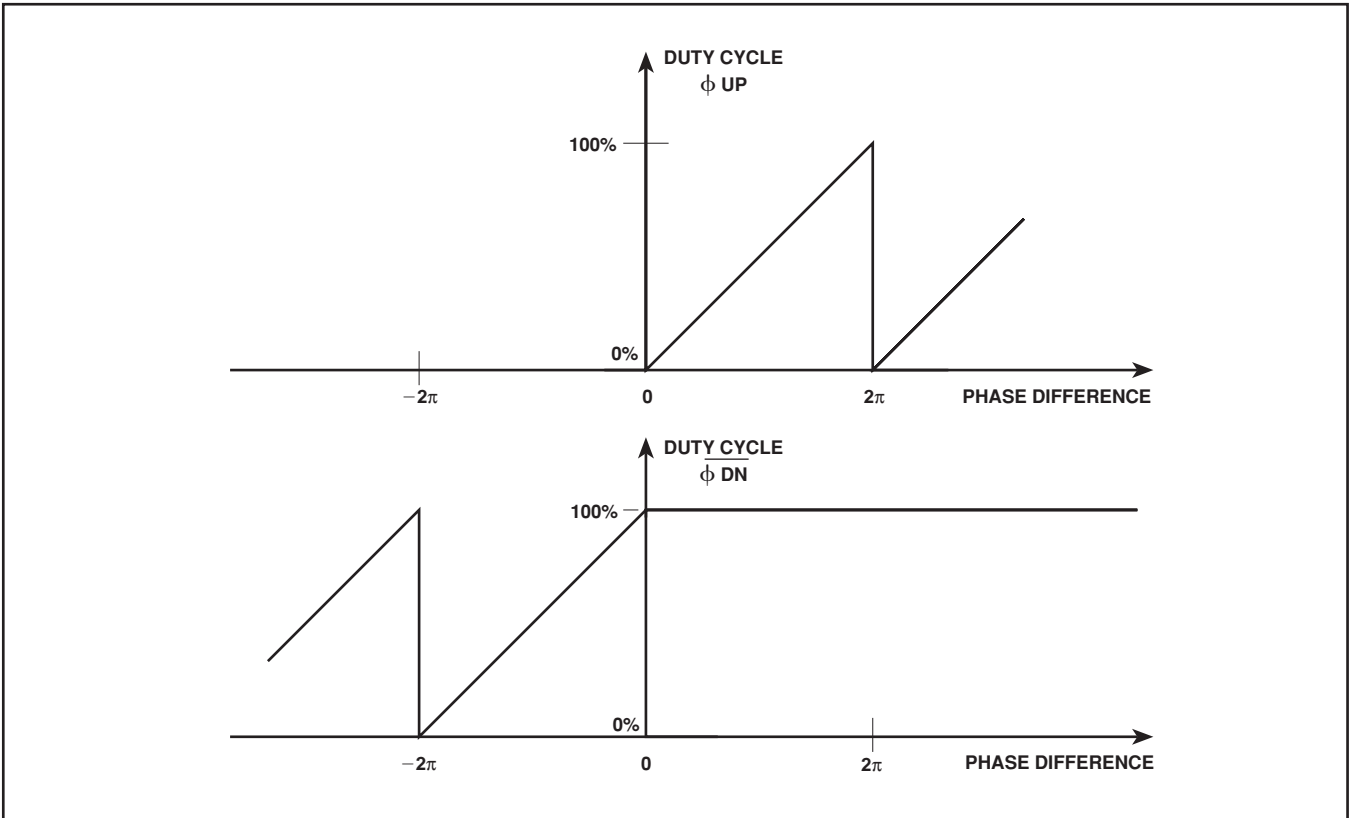


Fig. 7 Phase comparator output characteristics

Once the phase difference exceeds  $2\pi$ , the comparator will gain or slip one cycle and then try to lock on to the new zero phase difference. Note that very narrow pulses may be seen on the inactive phase comparator output at the end of the pulse on the active output, as shown in Fig. 6.

**Data Input and Control Register**

To control the synthesiser a simple three-line serial input is used with DATA, CLOCK and DATA TRANSFER signals. The data consists of 19 bits; the first three, DR2, DR1 and DR0, control the reference divider while the following sixteen, DF15

to DF0, control the prescaler and programmable divider. Until the synthesiser receives the DATA TRANSFER pulse, it will use the previously loaded data; on receiving the pulse it will switch rapidly to the new data.

**APPLICATIONS**

A simplified circuit for a synthesiser intended for VHF broadcast receiver applications is shown in Fig. 8. When the varicap line drive voltage necessary to tune the required band is greater than 5V, some form of level shifter such as the operational amplifier shown in Fig. 8 is required.

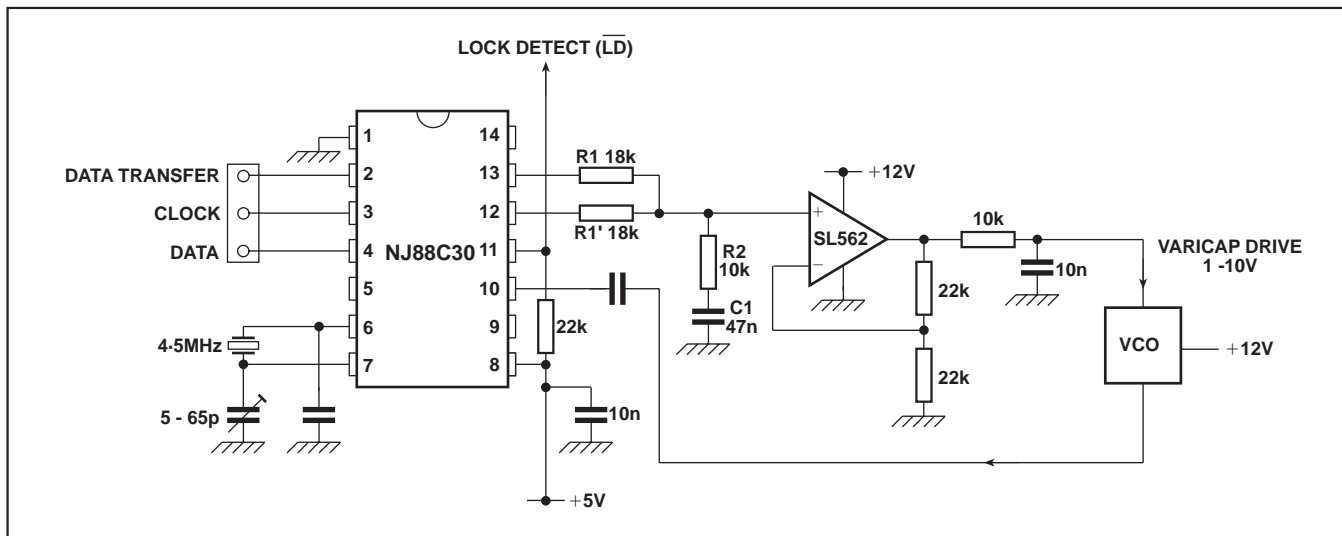


Fig.8. Typical application

**PROGRAMMING EXAMPLE**

**1. Maximum Frequency**

For a channel spacing (comparison frequency,  $f_{comp}$ ) of 5kHz when using a 10MHz crystal oscillator, the reference divider ratio will need to be 2000 (see Table 1). This is programmed as binary 100 (=  $4_{HEX}$ ) in the most significant three of the 19 bits (MSB programmed first).

To obtain the maximum VCO frequency of 200MHz the programmable divider ratio would be:

$$\frac{200 \times 10^6}{5 \times 10^3} = 40 \times 10^3 \text{ which is } 9C40_{HEX}$$

The program word would then be as shown in Table 2.

	DR			DF															
	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Binary	1	0	0	1	0	0	1	1	1	0	0	0	1	0	0	0	0	0	0
Hex	4			9				C				4				0			

Table 2 Maximum VCO frequency programming ( $f_{XTAL} = 10MHz$ ,  $f_{comp} = 5kHz$ )

**2. Minimum Frequency**

Using the same crystal frequency and channel spacing (10MHz, 5kHz), the lower limit of programmable divider ratio of

$240 = F0_{HEX}$  gives a minimum programmable VCO frequency of  $240 \times 5 \times 10^3 = 1.2MHz$ . The program word for this frequency is therefore as shown in Table 3.

	DR			DF															
	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Binary	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0
Hex	4			0				0				F				0			

Table 3 Minimum VCO frequency programming ( $f_{XTAL} = 10MHz$ ,  $f_{comp} = 5kHz$ )



HEADQUARTERS OPERATIONS

**GEC PLESSEY SEMICONDUCTORS**

Cheney Manor, Swindon,  
Wiltshire SN2 2QW, United Kingdom.  
Tel: (0793) 518000  
Fax: (0793) 518411

**GEC PLESSEY SEMICONDUCTORS**

P.O. Box 660017  
1500 Green Hills Road,  
Scotts Valley, California 95067-0017,  
United States of America.  
Tel: (408) 438 2900  
Fax: (408) 438 5576

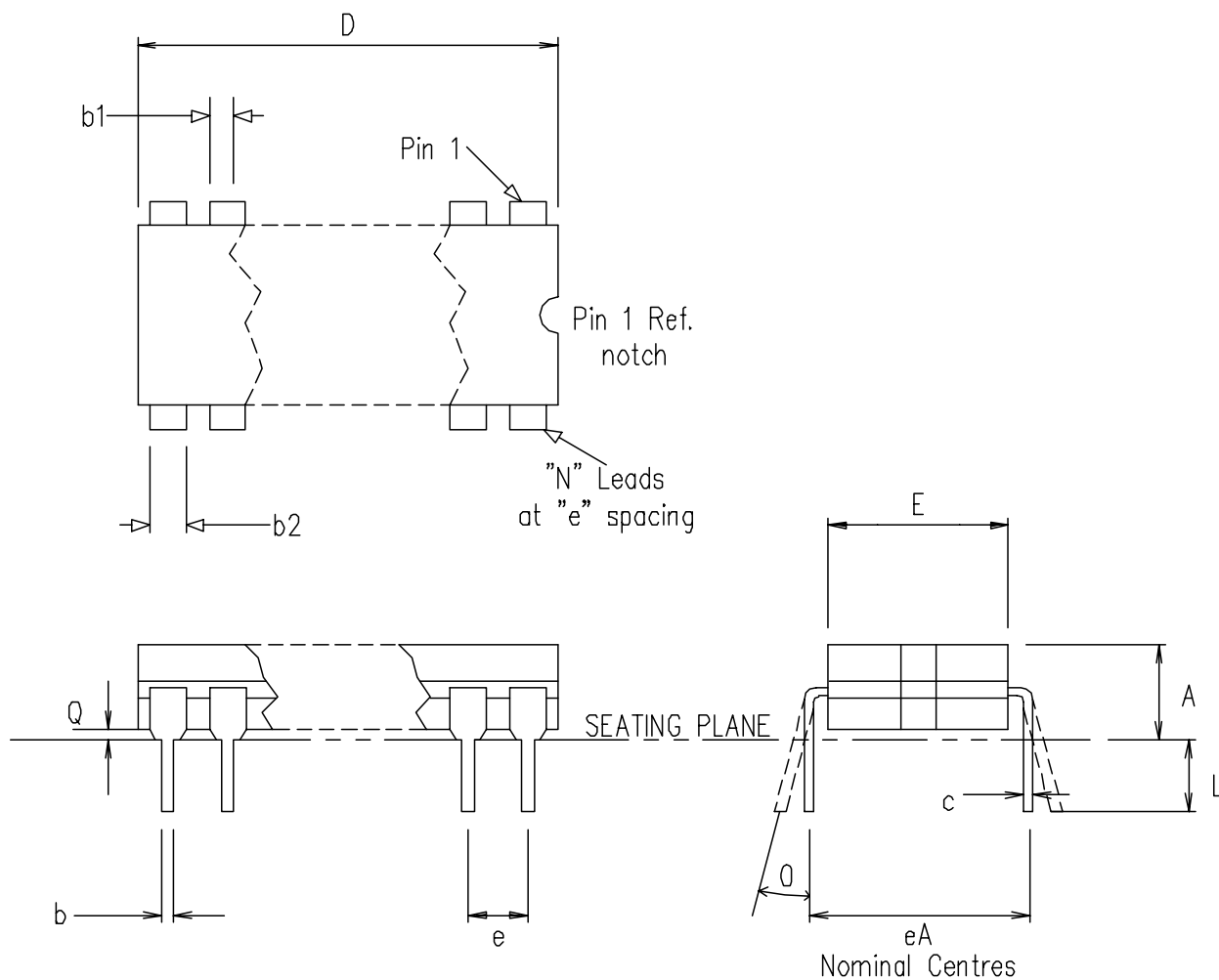
CUSTOMER SERVICE CENTRES

- **FRANCE & BENELUX** Les Ulis Cedex Tel: (1) 64 46 23 45 Tx: 602858F  
Fax : (1) 64 46 06 07
- **GERMANY** Munich Tel: (089) 3609 06-0 Tx: 523980 Fax : (089) 3609 06-55
- **ITALY** Milan Tel: (02) 66040867 Fax: (02) 66040993
- **JAPAN** Tokyo Tel: (03) 3296-0281 Fax: (03) 3296-0228
- **NORTH AMERICA Integrated Circuits and Microwave Products** Scotts Valley, USA  
Tel (408) 438 2900 Fax: (408) 438 7023.  
**Hybrid Products**, Farmingdale, USA Tel (516) 293 8686  
Fax: (516) 293 0061.
- **SOUTH EAST ASIA** Singapore Tel: (65) 3827708 Fax: (65) 3828872
- **SWEDEN** Stockholm, Tel: 46 8 702 97 70 Fax: 46 8 640 47 36
- **UNITED KINGDOM & SCANDINAVIA**  
Swindon Tel: (0793) 518510 Tx: 444410 Fax : (0793) 518582

These are supported by Agents and Distributors in major countries world-wide.

© GEC Plessey Semiconductors 1992 Publication No. DS3281 Issue No. 1.1 May 1992

This publication is issued to provide information only which (unless agreed by the Company in writing) may not be used, applied or reproduced for any purpose nor form part of any order or contract nor to be regarded as a representation relating to the products or services concerned. No warranty or guarantee express or implied is made regarding the capability, performance or suitability of any product or service. The Company reserves the right to alter without prior knowledge the specification, design or price of any product or service. Information concerning possible methods of use is provided as a guide only and does not constitute any guarantee that such methods of use will be satisfactory in a specific piece of equipment. It is the user's responsibility to fully determine the performance and suitability of any equipment using such information and to ensure that any publication or data used is up to date and has not been superseded. These products are not suitable for use in any medical products whose failure to perform may result in significant injury or death to the user. All products and materials are sold and services provided subject to the Company's conditions of sale, which are available on request.



Symbol	Altern. Dimensions in millimetres			Control Dimensions in inches		
	MIN	Nominal	MAX	MIN	Nominal	MAX
L	3.18		4.06	0.125		0.160
A			5.08			0.200
Q	0.51			0.020		
E	5.59		7.87	0.220		0.310
eA		7.62			0.300	
c	0.20		0.36	0.008		0.014
D			20.32			0.800
e	2.54 BSC.			0.100 BSC.		
b1	1.14		1.65	0.045		0.065
b	0.36		0.58	0.014		0.023
b2	0.73		1.12	0.029		0.044
Q			15°			15°
	Pin features					
N	14					
ND	7					
NE	0					
NOTE	RECTANGULAR					

This drawing supersedes 418/ED/39501/002 (Swindon)

© Mitel

ORIGINATING SITE: SWINDON

ISSUE	1				
ACN	201729				
DATE	20.NOV.96				
APPROVED					

MITEL SEMICONDUCTOR

Title: Outline drawing for  
14 Lead Cerdip (DG)

Drawing Number  
GPD00271





**For more information about all Zarlink products  
visit our Web Site at  
[www.zarlink.com](http://www.zarlink.com)**

Information relating to products and services furnished herein by Zarlink Semiconductor Inc. or its subsidiaries (collectively "Zarlink") is believed to be reliable. However, Zarlink assumes no liability for errors that may appear in this publication, or for liability otherwise arising from the application or use of any such information, product or service or for any infringement of patents or other intellectual property rights owned by third parties which may result from such application or use. Neither the supply of such information or purchase of product or service conveys any license, either express or implied, under patents or other intellectual property rights owned by Zarlink or licensed from third parties by Zarlink, whatsoever. Purchasers of products are also hereby notified that the use of product in certain ways or in combination with Zarlink, or non-Zarlink furnished goods or services may infringe patents or other intellectual property rights owned by Zarlink.

This publication is issued to provide information only and (unless agreed by Zarlink in writing) may not be used, applied or reproduced for any purpose nor form part of any order or contract nor to be regarded as a representation relating to the products or services concerned. The products, their specifications, services and other information appearing in this publication are subject to change by Zarlink without notice. No warranty or guarantee express or implied is made regarding the capability, performance or suitability of any product or service. Information concerning possible methods of use is provided as a guide only and does not constitute any guarantee that such methods of use will be satisfactory in a specific piece of equipment. It is the user's responsibility to fully determine the performance and suitability of any equipment using such information and to ensure that any publication or data used is up to date and has not been superseded. Manufacturing does not necessarily include testing of all functions or parameters. These products are not suitable for use in any medical products whose failure to perform may result in significant injury or death to the user. All products and materials are sold and services provided subject to Zarlink's conditions of sale which are available on request.

Purchase of Zarlink's I<sup>2</sup>C components conveys a licence under the Philips I<sup>2</sup>C Patent rights to use these components in and I<sup>2</sup>C System, provided that the system conforms to the I<sup>2</sup>C Standard Specification as defined by Philips.

Zarlink, ZL and the Zarlink Semiconductor logo are trademarks of Zarlink Semiconductor Inc.

Copyright Zarlink Semiconductor Inc. All Rights Reserved.

**TECHNICAL DOCUMENTATION - NOT FOR RESALE**

---