

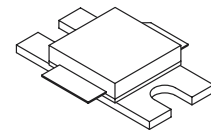
The RF MOSFET Line
RF Power Field Effect Transistors
N-Channel Enhancement-Mode Lateral MOSFETs

MRF21030R3
MRF21030SR3

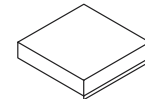
Designed for PCN and PCS base station applications with frequencies from 2.0 to 2.2 GHz. Suitable for FM, TDMA, CDMA and multicarrier amplifier applications. To be used in Class AB for PCN-PCS/cellular radio and WLL applications.

- Wideband CDMA Performance: -45 dB ACPR @ 4.096 MHz, 28 Volts
Output Power — 3.5 Watts
Power Gain — 14 dB
Efficiency — 15%
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 10:1 VSWR, @ 28 Vdc, 2.11 GHz, 30 Watts CW Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- In Tape and Reel. R3 Suffix = 250 Units per 32 mm, 13 Inch Reel.

2.2 GHz, 30 W, 28 V
LATERAL N-CHANNEL
RF POWER MOSFETs



CASE 465E-03, STYLE 1
NI-400
MRF21030R3



CASE 465F-03, STYLE 1
NI-400S
MRF21030SR3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	65	Vdc
Gate-Source Voltage	V_{GS}	-0.5, +15	Vdc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	83.3 0.48	Watts W/ $^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +200	$^\circ\text{C}$
Operating Junction Temperature	T_J	200	$^\circ\text{C}$

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	2 (Minimum)
Machine Model	M3 (Minimum)

THERMAL CHARACTERISTICS

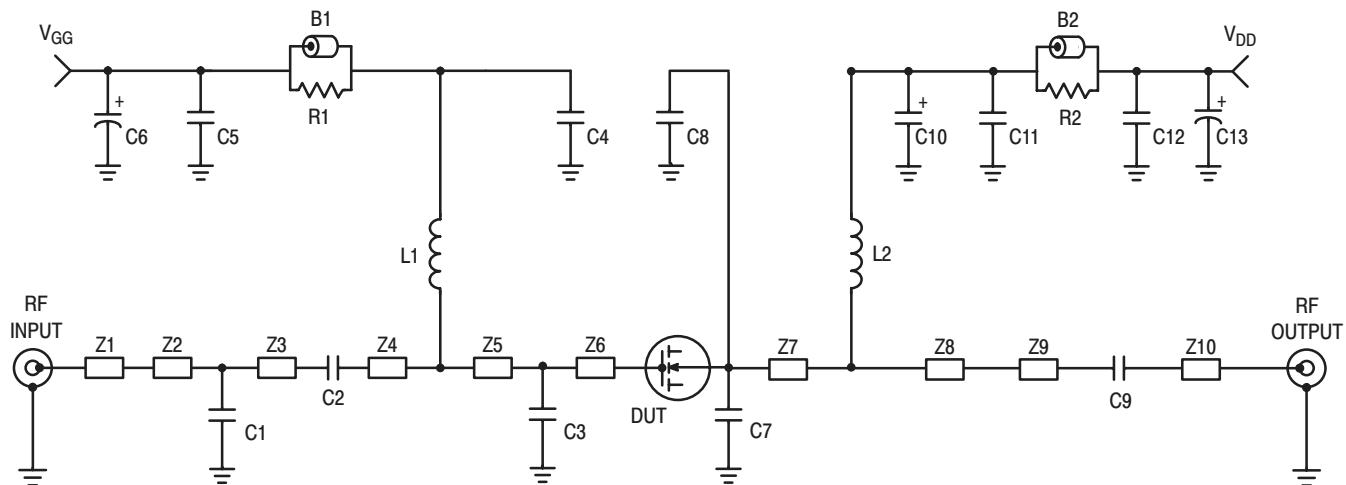
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.1	$^\circ\text{C}/\text{W}$

NOTE - **CAUTION** - MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage ($V_{GS} = 0\text{ Vdc}$, $I_D = 20\ \mu\text{A}$)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current ($V_{DS} = 28\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$)	I_{DSS}	—	—	1	μAdc
Gate–Source Leakage Current ($V_{GS} = 5\text{ Vdc}$, $V_{DS} = 0\text{ Vdc}$)	I_{GSS}	—	—	1	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage ($V_{DS} = 10\text{ Vdc}$, $I_D = 100\ \mu\text{Adc}$)	$V_{GS(th)}$	2	3	4	Vdc
Gate Quiescent Voltage ($V_{DS} = 28\text{ Vdc}$, $I_D = 250\text{ mA}$)	$V_{GS(Q)}$	2	3.3	4.5	Vdc
Drain–Source On–Voltage ($V_{GS} = 10\text{ Vdc}$, $I_D = 1\text{ Adc}$)	$V_{DS(on)}$	—	0.29	0.4	Vdc
Forward Transconductance ($V_{DS} = 10\text{ Vdc}$, $I_D = 1\text{ Adc}$)	g_{fs}	—	2	—	S
DYNAMIC CHARACTERISTICS					
Input Capacitance (Including Input Matching Capacitor in Package) (1) ($V_{DS} = 28\text{ Vdc}$, $V_{GS} = 0$, $f = 1\text{ MHz}$)	C_{iss}	—	98.5	—	pF
Output Capacitance (1) ($V_{DS} = 28\text{ Vdc}$, $V_{GS} = 0$, $f = 1\text{ MHz}$)	C_{oss}	—	37	—	pF
Reverse Transfer Capacitance ($V_{DS} = 28\text{ Vdc}$, $V_{GS} = 0$, $f = 1\text{ MHz}$)	C_{rss}	—	1.3	—	pF
FUNCTIONAL TESTS (In Motorola Test Fixture, 50 ohm system)					
Two–Tone Common–Source Amplifier Power Gain ($V_{DD} = 28\text{ Vdc}$, $P_{out} = 30\text{ W PEP}$, $I_{DQ} = 250\text{ mA}$, $f_1 = 2140.0\text{ MHz}$, $f_2 = 2140.1\text{ MHz}$)	G_{ps}	—	13	—	dB
Two–Tone Drain Efficiency ($V_{DD} = 28\text{ Vdc}$, $P_{out} = 30\text{ W PEP}$, $I_{DQ} = 250\text{ mA}$, $f_1 = 2140.0\text{ MHz}$, $f_2 = 2140.1\text{ MHz}$)	η	—	33	—	%
3rd Order Intermodulation Distortion ($V_{DD} = 28\text{ Vdc}$, $P_{out} = 30\text{ W PEP}$, $I_{DQ} = 250\text{ mA}$, $f_1 = 2140.0\text{ MHz}$, $f_2 = 2140.1\text{ MHz}$)	IMD	—	–30	—	dBc
Input Return Loss ($V_{DD} = 28\text{ Vdc}$, $P_{out} = 30\text{ W PEP}$, $I_{DQ} = 250\text{ mA}$, $f_1 = 2140.0\text{ MHz}$, $f_2 = 2140.1\text{ MHz}$)	IRL	—	–13	—	dB
Two–Tone Common–Source Amplifier Power Gain ($V_{DD} = 28\text{ Vdc}$, $P_{out} = 30\text{ W PEP}$, $I_{DQ} = 250\text{ mA}$, $f_1 = 2110.0\text{ MHz}$, $f_2 = 2110.1\text{ MHz}$ and $f_1 = 2170.0\text{ MHz}$, $f_2 = 2170.1\text{ MHz}$)	G_{ps}	12	13	—	dB
Two–Tone Drain Efficiency ($V_{DD} = 28\text{ Vdc}$, $P_{out} = 30\text{ W PEP}$, $I_{DQ} = 250\text{ mA}$, $f_1 = 2110.0\text{ MHz}$, $f_2 = 2110.1\text{ MHz}$ and $f_1 = 2170.0\text{ MHz}$, $f_2 = 2170.1\text{ MHz}$)	η	31	33	—	%
3rd Order Intermodulation Distortion ($V_{DD} = 28\text{ Vdc}$, $P_{out} = 30\text{ W PEP}$, $I_{DQ} = 250\text{ mA}$, $f_1 = 2110.0\text{ MHz}$, $f_2 = 2110.1\text{ MHz}$ and $f_1 = 2170.0\text{ MHz}$, $f_2 = 2170.1\text{ MHz}$)	IMD	—	–30	–27.5	dBc
Input Return Loss ($V_{DD} = 28\text{ Vdc}$, $P_{out} = 30\text{ W PEP}$, $I_{DQ} = 250\text{ mA}$, $f_1 = 2110.0\text{ MHz}$, $f_2 = 2110.1\text{ MHz}$ and $f_1 = 2170.0\text{ MHz}$, $f_2 = 2170.1\text{ MHz}$)	IRL	—	–13	–9	dB
Output Mismatch Stress ($V_{DD} = 28\text{ Vdc}$, $P_{out} = 30\text{ W CW}$, $I_{DQ} = 250\text{ mA}$, $f = 2110\text{ MHz}$, $V_{SWR} = 10:1$, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power Before and After Test			

(1) Part is internally matched both on input and output.



B1, B2	Short Ferrite Beads	Z1	0.153" x 0.087" Microstrip
C1	1 pF Chip Capacitor	Z2	0.509" x 0.156" Microstrip
C2	4.7 pF Chip Capacitor	Z3	0.572" x 0.087" Microstrip
C3	0.5 pF Chip Capacitor	Z4	0.509" x 0.232" Microstrip
C4	3.9 pF Chip Capacitor	Z5	0.277" x 0.143" Microstrip
C5, C12	0.1 μ F Chip Capacitors	Z6	0.200" x 0.305" Microstrip
C6, C13	470 μ F, 63 V Electrolytic Chip Capacitors	Z7	0.200" x 0.511" Microstrip
C7, C8	0.3 pF Chip Capacitors	Z8	0.510" x 0.328" Microstrip
C9	3.6 pF Chip Capacitor	Z9	0.608" x 0.081" Microstrip
C10	22 μ F Tantalum Chip Capacitor	Board	0.030" Glass Teflon [®] , TLX8-0300
C11	5.1 pF Chip Capacitor		Taconix ($\epsilon_r = 2.55$)
L1, L2	12.5 nH Inductors		
R1, R2	12 Ω Chip Resistors (1206)		

Figure 1. MRF21030 Test Circuit Schematic

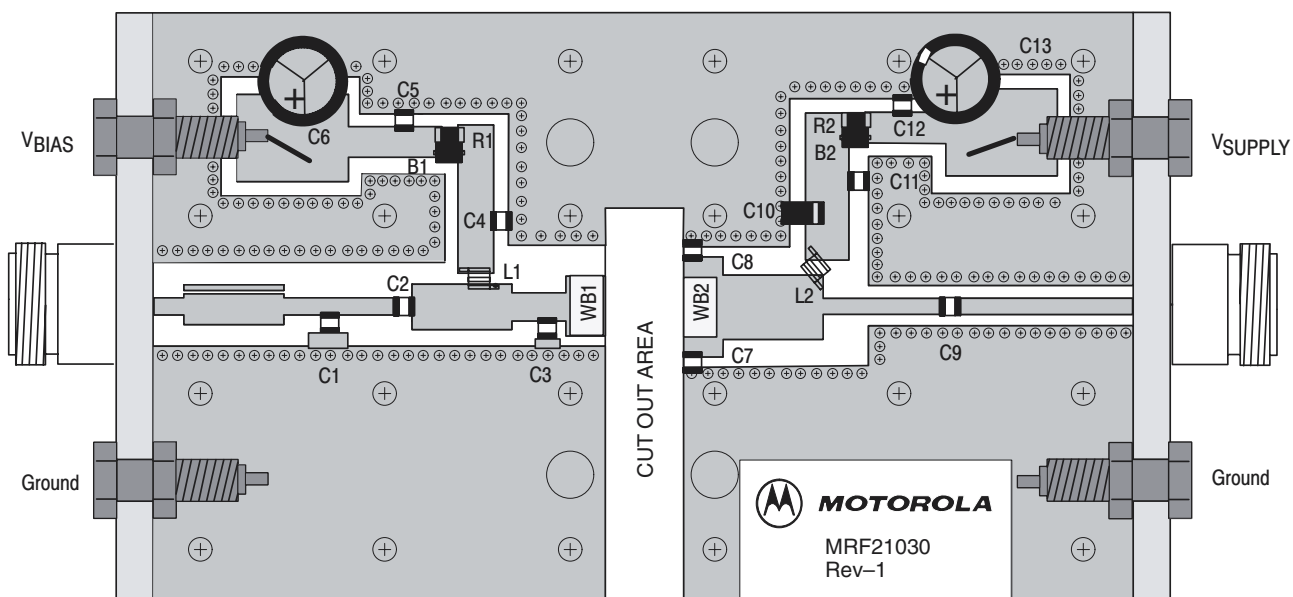


Figure 2. MRF21030 Test Circuit Component Layout

TYPICAL CHARACTERISTICS

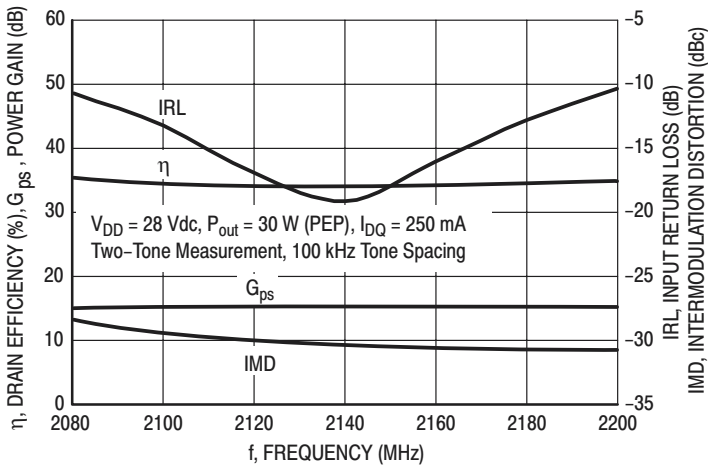


Figure 3. Class AB Broadband Circuit Performance

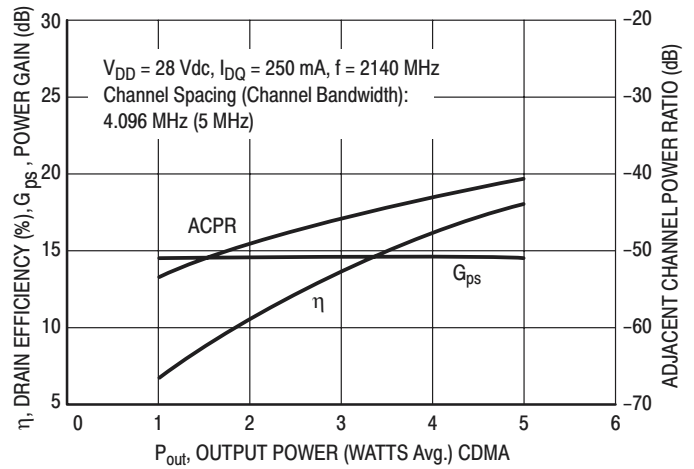


Figure 4. CDMA ACPR, Power Gain and Drain Efficiency versus Output Power

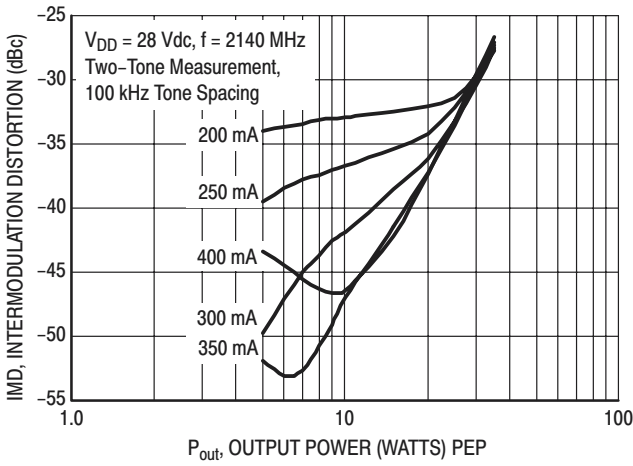


Figure 5. Intermodulation Distortion versus Output Power

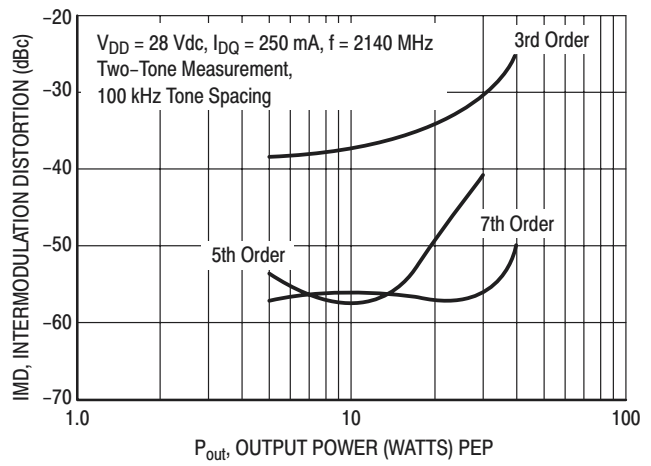


Figure 6. Intermodulation Distortion Products versus Output Power

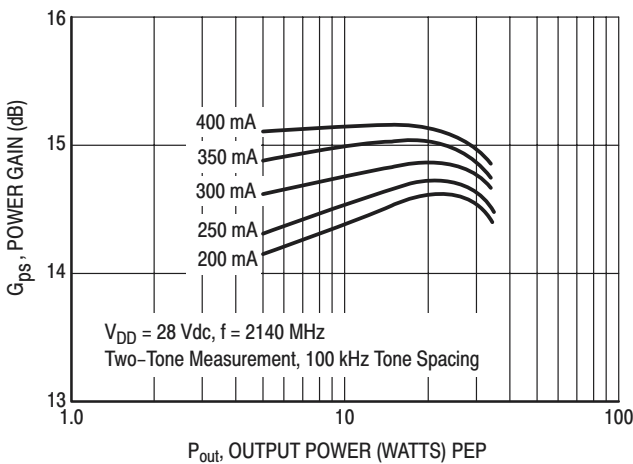


Figure 7. Power Gain versus Output Power

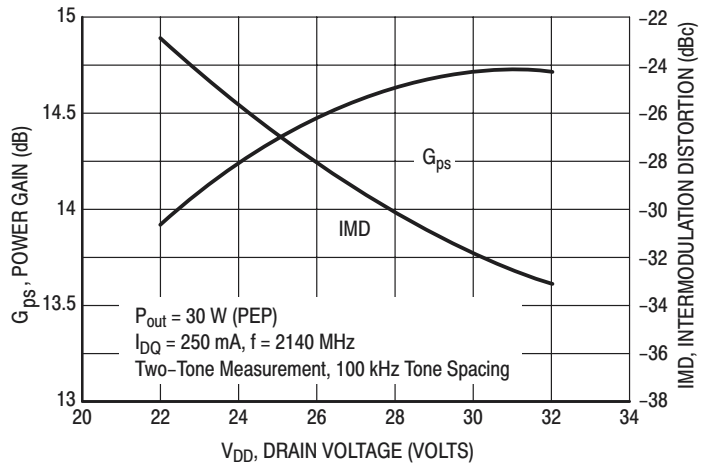
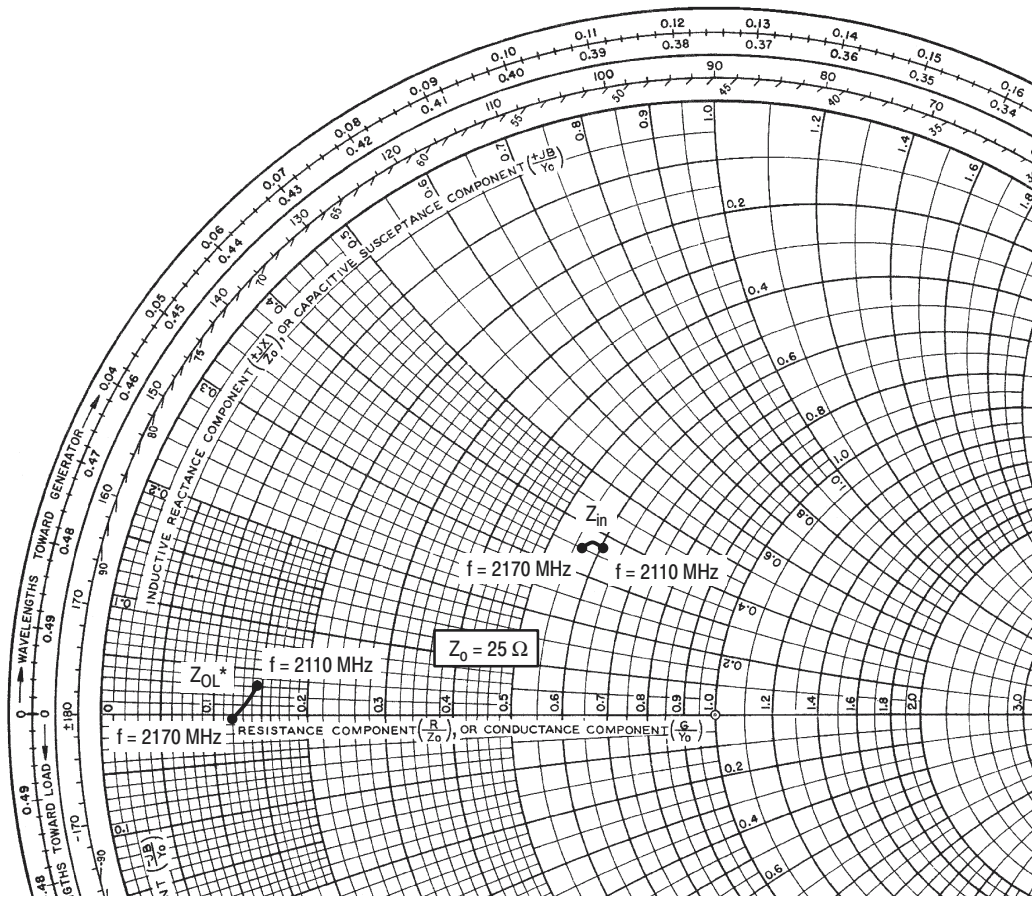


Figure 8. Power Gain and Intermodulation Distortion versus Supply Voltage



$V_{DD} = 28 \text{ V}$, $I_{DQ} = 250 \text{ mA}$, $P_{out} = 30 \text{ W PEP}$

f MHz	Z_{in} Ω	Z_{OL}^* Ω
2110	$15.3 + j9.4$	$3.7 + j0.78$
2140	$14.6 + j9.4$	$3.4 + j0.37$
2170	$14.3 + j8.8$	$3.0 - j0.13$

Z_{in} = Complex conjugate of source impedance.

Z_{OL}^* = Complex conjugate of the optimum load impedance at a given output power, voltage, IMD, bias current and frequency.

Note: Z_{OL}^* was chosen based on tradeoffs between gain, output power, drain efficiency and intermodulation distortion.

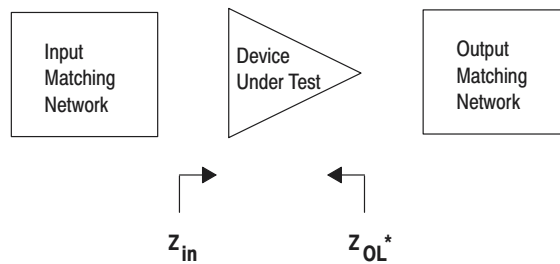
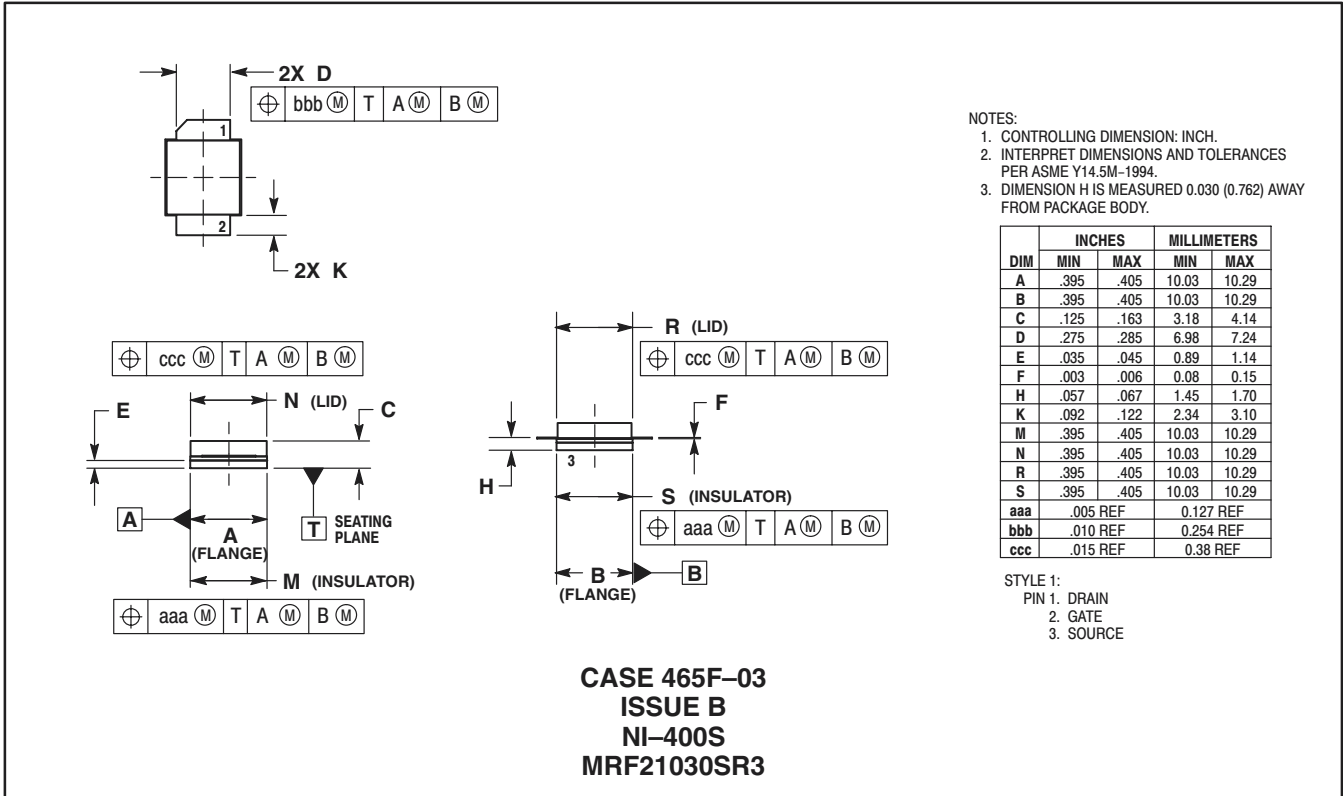
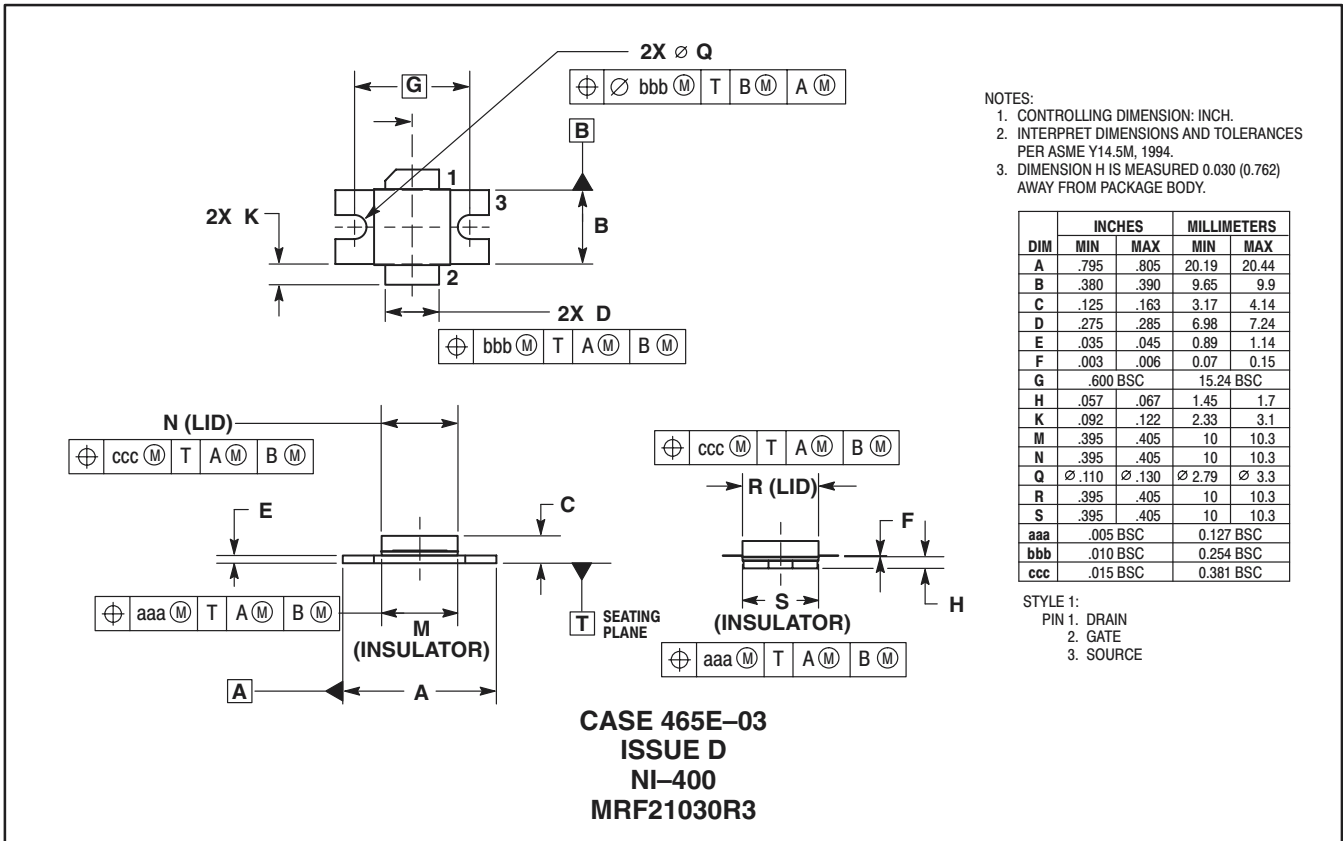



Figure 9. Series Equivalent Input and Output Impedance

NOTES

PACKAGE DIMENSIONS



Motorola reserves the right to make changes without further notice to any products herein. Motorola makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Motorola assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters which may be provided in Motorola data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. Motorola does not convey any license under its patent rights nor the rights of others. Motorola products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Motorola product could create a situation where personal injury or death may occur. Should Buyer purchase or use Motorola products for any such unintended or unauthorized application, Buyer shall indemnify and hold Motorola and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Motorola was negligent regarding the design or manufacture of the part. Motorola, Inc. Motorola, Inc. is an Equal Opportunity/Affirmative Action Employer. MOTOROLA and the  logo are registered in the US Patent & Trademark Office. All other product or service names are the property of their respective owners.

© Motorola, Inc. 2002.

How to reach us:

USA/EUROPE/Locations Not Listed: Motorola Literature Distribution; P.O. Box 5405, Denver, Colorado 80217. 1-303-675-2140 or 1-800-441-2447

JAPAN: Motorola Japan Ltd.; SPS, Technical Information Center, 3-20-1, Minami-Azabu. Minato-ku, Tokyo 106-8573 Japan. 81-3-3440-3569

ASIA/PACIFIC: Motorola Semiconductors H.K. Ltd.; Silicon Harbour Centre, 2 Dai King Street, Tai Po Industrial Estate, Tai Po, N.T., Hong Kong. 852-26668334

Technical Information Center: 1-800-521-6274

HOME PAGE: <http://www.motorola.com/semiconductors/>



This datasheet has been download from:

www.datasheetcatalog.com

Datasheets for electronics components.