

SONY CXK58257P/SP/M 70L/85L/10L/12L
70LL/85LL/10LL/12LL

32768-word × 8 bit High Speed CMOS Static RAM T-46-23-14

Description

CXK58257P/SP/M is a 262,144 bits high speed CMOS static RAM organized as 32,768 words by 8 bits and operates from a single 5V supply. This device is suitable for use in high speed and low power applications in which battery back up for nonvolatility is required.

Features

- Fast access time: (Access time)
 - CXK58257P/SP/M-70L, 70LL 70ns (Max.)
 - CXK58257P/SP/M-85L, 85LL 85ns (Max.)
 - CXK58257P/SP/M-10L, 10LL 100ns (Max.)
 - CXK58257P/SP/M-12L, 12LL 120ns (Max.)
- Low power operation:
 - CXK58257P/SP/M-70LL, 85LL, 10LL, 12LL:
Standby/Operation: 5 μW (Typ.)/40 mW (Typ.)
 - CXK58257P/SP/M-70L, 85L, 10L, 12L:
Standby/Operation: 10 μW (Typ.)/40 mW (Typ.)
- Single +5V supply: +5V ±10%
- Fully static memory... No clock or timing strobe required
- Equal access and cycle time
- Common data input and output: three state output
- Directly TTL compatible: All inputs and outputs
- Low voltage data retention: 2.0V (Min.)
- Available in 28pin 600-mil DIP, 300-mil DIP and 450-mil SOP

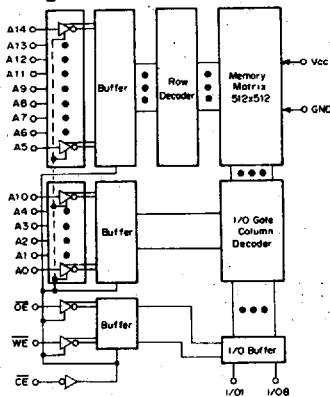
Function

32768-word × 8 bit static RAM

Structure

Silicon gate CMOS IC

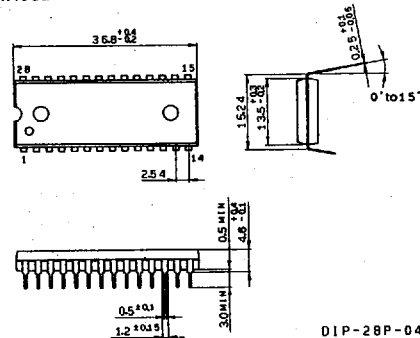
Block Diagram



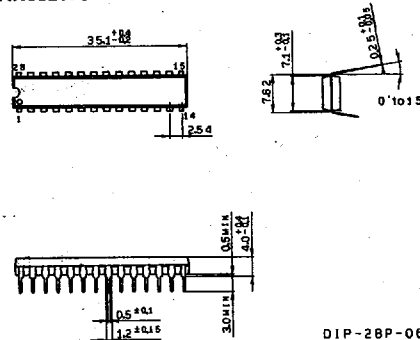
Package Outline

Unit: mm

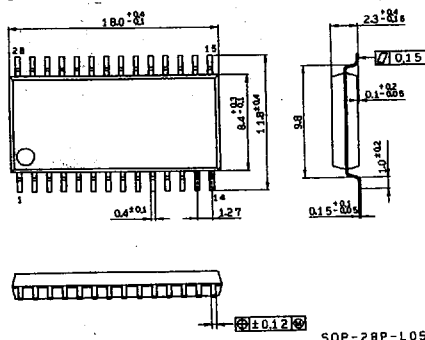
CXK58257P 28 Pin DIP (Plastic)



CXK58257SP 28 Pin DIP (Plastic)



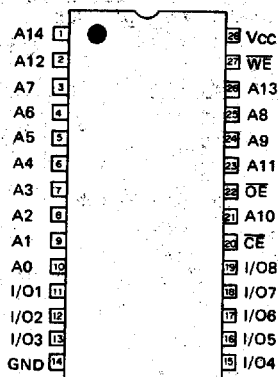
CXK58257M 28 Pin SOP (Plastic)



Pin Configuration (Top View)

Pin Description

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Symbol	Description
A0 to A14	Address input
I/O1 to I/O8	Data input output
\overline{CE}	Chip enable input
\overline{WE}	Write enable input
\overline{OE}	Output enable input
Vcc	Power supply
GND	Ground

Absolute Maximum Ratings

(Ta=25°C, GND=0V)

Item	Symbol	Rating	Unit
Supply voltage	Vcc	-0.5 to +7.0	V
Input voltage	V _{IN}	-0.5* to Vcc+0.5	V
Input and output voltage	V _{IO}	-0.5* to Vcc+0.5	V
Allowable power dissipation	P _D CXK58257P/SP	1.0	W
	CXK58257M	0.7	
Operating temperature	T _{opr}	0 to +70	°C
Storage temperature	T _{stg}	-55 to +150	°C
Soldering temperature	T _{solder}	260.10	°C·sec.

*Note) V_{IN}, V_{IO}=-3.0V Min. for pulse width less than 50 ns.

Truth Table

\overline{CE}	\overline{OE}	\overline{WE}	Mode	I/O1 to I/O8	Vcc Current
H	X	X	Not Selected	High Z	I _{SB1} , I _{SB2}
L	H	H	Output Disable	High Z	I _{CC1} , I _{CC2}
L	L	H	Read	Data out	I _{CC1} , I _{CC2}
L	X	L	Write	Data in	I _{CC1} , I _{CC2}

Note) X: "H" or "L"

DC Recommended Operating Conditions (Ta=0 to +70°C, GND=0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	Vcc	4.5	5.0	5.5	V
Input high voltage	V _{IH}	2.2	-	Vcc+0.3	V
Input low voltage	V _{IL}	-0.3*	-	0.8	V

*Note) V_{IL}=-3.0V Min. for pulse width less than 50 ns.

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Electrical Characteristics

DC and operating characteristics

(Vcc=5V±10%, GND=0V, Ta=0 to +70°C)

Item	Symbol	Test condition	CXK58257P/SP/M -70L/85L/10L/12L			CXK58257P/SP/M -70LL 85LL/10LL/12LL			Unit	
			Min.	Typ.*	Max.	Min.	Typ.*	Max.		
Input leakage current	I _I	V _{IN} =GND to V _{CC}	-0.5	-	0.5	-0.5	-	0.5	μA	
Output leakage current	I _O	$\overline{CE}=V_{IH}$ or $\overline{OE}=V_{IH}$ V _{I/O} =GND to V _{CC}	-0.5	-	0.5	-0.5	-	0.5	μA	
Operating power supply current	I _{CC1}	$\overline{CE}=V_{IL}$ V _{IN} =V _{IH} or V _{IL} I _{OUT} =0mA	-	8	15	-	8	15	mA	
		$\overline{CE} \leq 0.2V$ V _{IN} ≤ 0.2V or ≥ V _{CC} - 0.2V	-	3	7	-	3	7	mA	
Average operating current	I _{CC2}	Min. cycle Duty=100% I _{OUT} =0mA	70L/70LL	-	45	70	-	45	70	mA
			85L/85LL	-	40	70	-	40	70	mA
			10L/10LL	-	35	70	-	35	70	mA
			12L/12LL	-	30	70	-	30	70	mA
Standby current	IS81	$\overline{CE} \geq V_{CC} - 0.2V$	-	0.002	0.1	-	0.001	0.05	mA	
	IS82	$\overline{CE} = V_{IH}$	-	0.2	2	-	0.2	2	mA	
Output high voltage	V _{OH}	I _{OH} = -1.0mA	2.4	-	-	2.4	-	-	V	
Output low voltage	V _{OL}	I _{OL} = 2.1mA	-	-	0.4	-	-	0.4	V	

* Note) Vcc=5V, Ta=25°C

Capacitance

(Ta=25°C, f=1 MHz)

Item	Symbol	Test Condition	Min.	Max.	Unit
Input capacitance	C _{IN}	V _{IN} =0V	-	6	pF
Input/output capacitance	C _{I/O}	V _{I/O} =0V	-	8	pF

Note) This parameter is sampled and is not 100% tested.

AC Characteristics

• AC test conditions (Vcc=5V±10%, Ta=0 to +70°C)

Item	Condition	
Input pulse high level	V _{IH} =2.2V	
Input pulse low level	V _{IL} =0.8V	
Input rise time	t _r =5ns	
Input fall time	t _f =5ns	
Input and output reference level	1.5V	
Output load	85L/85LL/10L/10LL 12L/12LL	C _L * = 100pF, 1TTL
	70L/70LL	C _L * = 30pF, 1TTL

* C_L includes scope and jig capacitances.

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• Read cycle

Item	Symbol	CXK58257 P/SP/M -70L/70LL		CXK58257 P/SP/M -85L/85LL		CXK58257 P/SP/M -10L/10LL		CXK58257 P/SP/M -12L/12LL		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
		Read cycle time	trc	70	-	85	-	100	-	
Address access time	tAA	-	70	-	85	-	100	-	120	ns
Chip enable access time	tCO	-	70	-	85	-	100	-	120	ns
Output enable to output valid	toE	-	35	-	45	-	50	-	60	ns
Output hold from address change	toH	5	-	5	-	10	-	10	-	ns
Chip enable to output in low Z (\overline{CE})	tlZ	10	-	10	-	10	-	10	-	ns
Output enable to output in low Z (\overline{OE})	tolZ	5	-	5	-	5	-	5	-	ns
Chip disable to output in high Z (\overline{CE})	thZ*	0	30	0	30	0	35	0	40	ns
Output disable to output in high Z (\overline{OE})	toHZ*	0	30	0	30	0	35	0	40	ns

*Note) thZ and toHZ are defined as the time at which the outputs become the high impedance state and are not referred to output voltage levels.

• Write cycle

Item	Symbol	CXK58257 P/SP/M -70L/70LL		CXK58257 P/SP/M -85L/85LL		CXK58257 P/SP/M -10L/10LL		CXK58257 P/SP/M -12L/12LL		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
		Write cycle time	tWC	70	-	85	-	100	-	
Address valid to end of write	tAW	65	-	75	-	80	-	100	-	ns
Chip enable to end of write	tCW	65	-	75	-	80	-	100	-	ns
Data to write time overlap	tdW	30	-	40	-	40	-	50	-	ns
Data hold from write time	tdH	0	-	0	-	0	-	0	-	ns
Write pulse width	tWP	55	-	60	-	70	-	80	-	ns
Address setup time	tAS	0	-	0	-	0	-	0	-	ns
Write recovery time (\overline{WE})	tWR	0	-	0	-	0	-	0	-	ns
Write recovery time (\overline{CE})	tWR1	0	-	0	-	0	-	0	-	ns
Output active from end of write	tOW	5	-	5	-	10	-	10	-	ns
Write to output in high Z	tWHZ*	0	30	0	30	0	30	0	30	ns

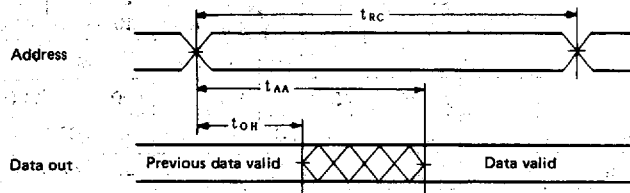
*Note) tWHZ is defined as the time at which the outputs become the high impedance state and are not referred to output voltage levels.

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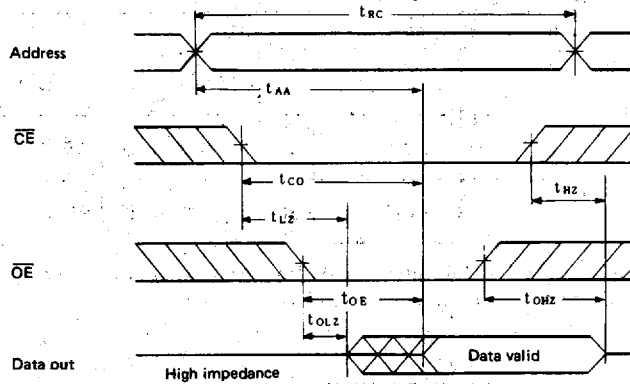
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Timing Waveform

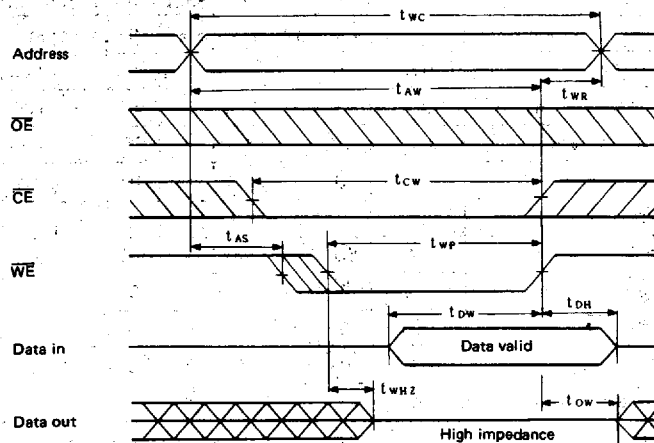
- Read cycle (1): $\overline{CE}=\overline{OE}=V_{IL}, \overline{WE}=V_{IH}$



- Read cycle (2): $\overline{WE}=V_{IH}$

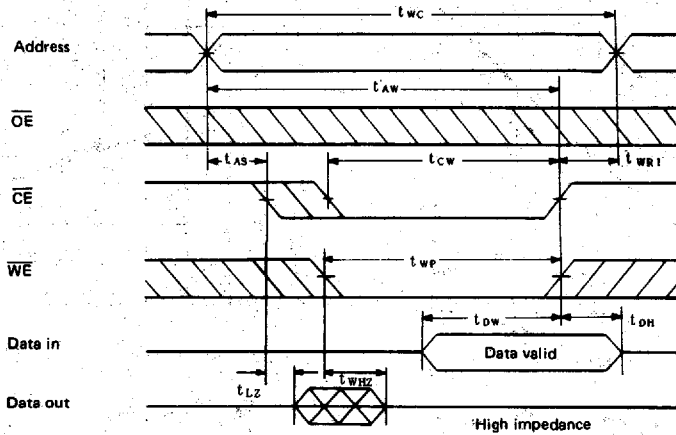


- Write cycle (1): \overline{WE} control



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• Write cycle (2): \overline{CE} control



During I/O pins are in the output state, the data input signals of opposite phase to the output must not be applied.

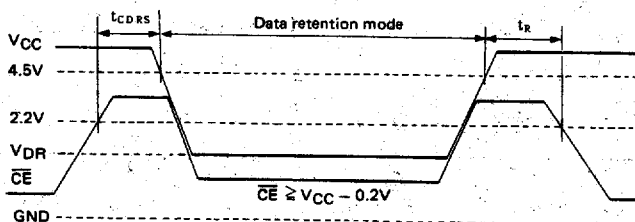
Data Retention Characteristics

($T_a=0$ to 70°C)

Item	Symbol	Test condition	CXK58257P/SP/M -70L/85L/10L/12L			CXK58257P/SP/M -70LL 85LL/10LL/12LL			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Data retention voltage	V_{DR}	$\overline{CE} \geq V_{CC} - 0.2V$	2.0	-	5.5	2.0	-	5.5	V
Data retention current	I_{CCDR1}	$V_{CC}=3.0V$	-	1	50	-	0.4	10	μA
		$\overline{CE} \geq 2.8V$	-	-	-	-	0.4	5	
		25°C	-	-	-	-	0.4	1	
	I_{CCDR2}	$V_{CC}=2.0$ to $5.5V$ $\overline{CE} \geq V_{CC} - 0.2V$	-	0.002	0.1	-	0.001	0.05	mA
Data retention setup time	t_{CDRS}	Chip disable to data retention mode	0	-	-	0	-	-	ns
Recovery time	t_r		t_{rc}^*	-	-	t_{rc}^*	-	-	ns

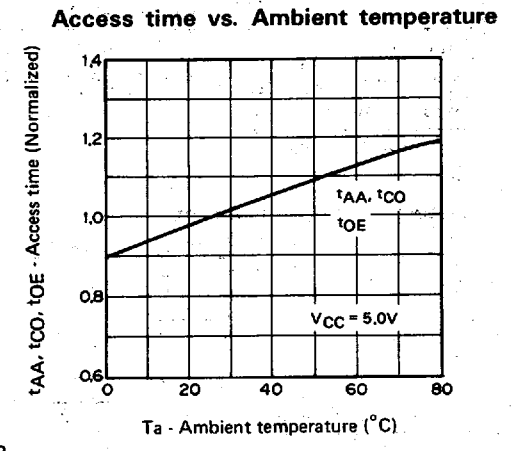
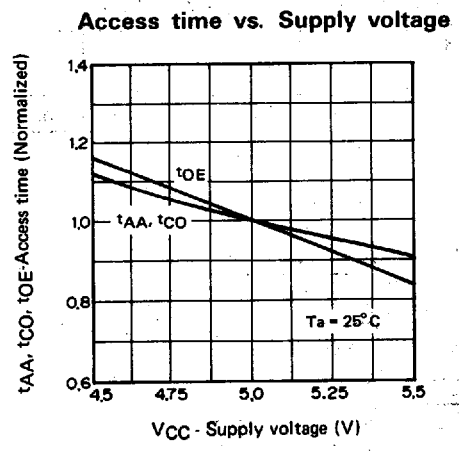
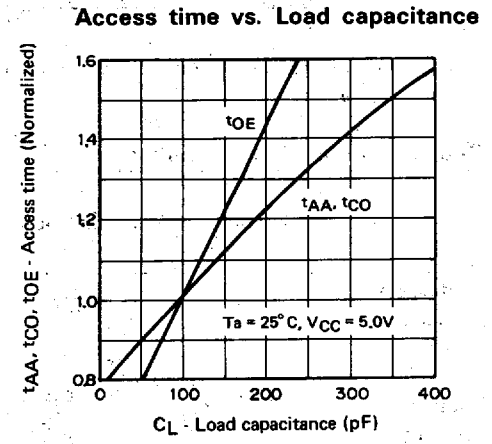
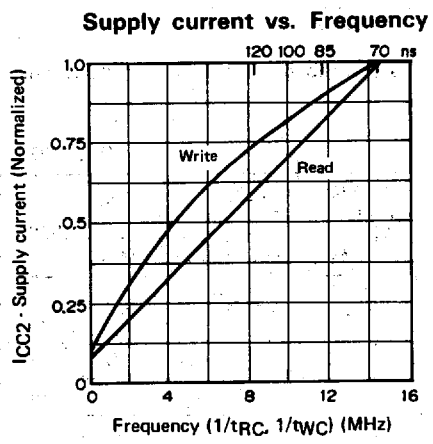
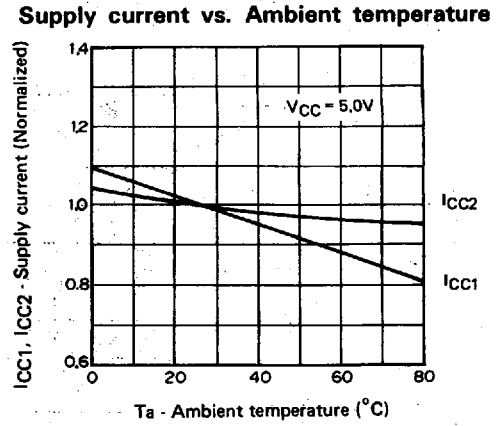
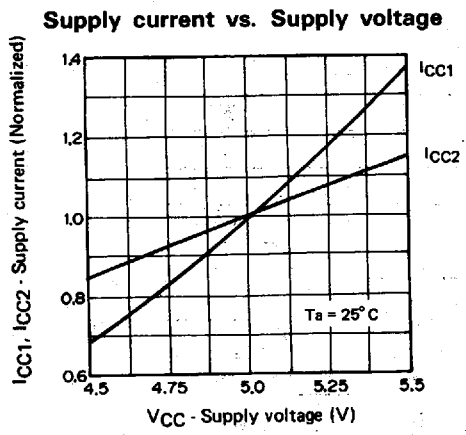
* t_{rc} : Read cycle time

• Data-retention waveform



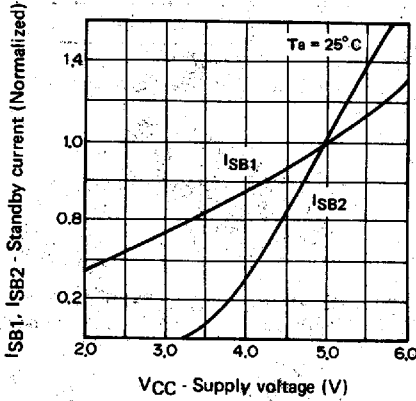
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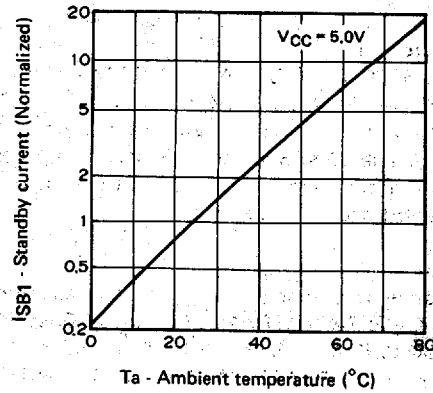


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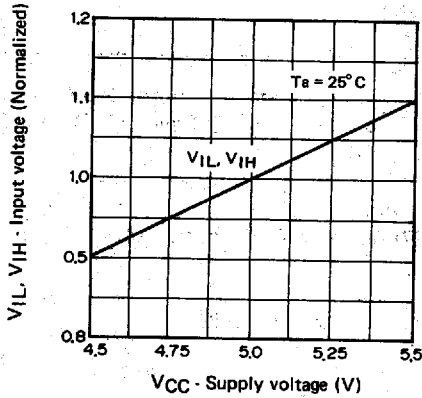
Standby current vs. Supply voltage



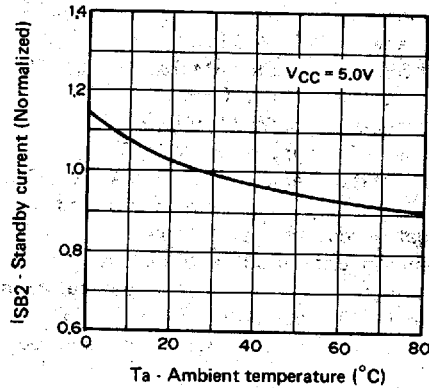
Standby current vs. Ambient temperature



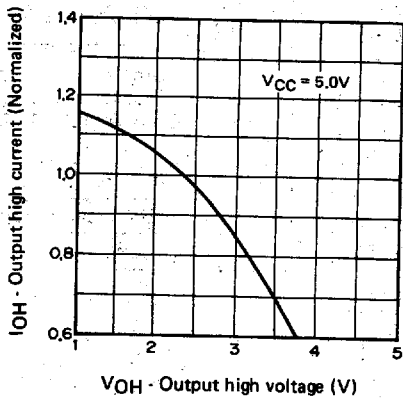
Input voltage vs. Supply voltage



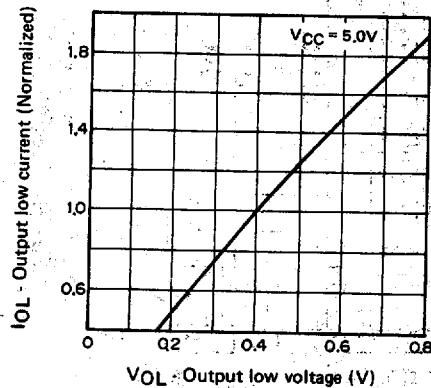
Standby current vs. Ambient temperature



Output high current vs. Output high voltage



Output low current vs. Output low voltage



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