Ordering number : EN5157C

CMOS LSI

LC72336, 72338

Single-Chip Microcontrollers with Built-In LCD Driver and PLL Circuits

Overview

The LC72336 and LC72338 are single-chip microcontrollers for use in electronic tuners. These products include on chip a PLL circuit that can operate at up to 150 MHz and 1/3 duty LCD drivers. They feature a highly efficient instruction set and powerful hardware.

Functions

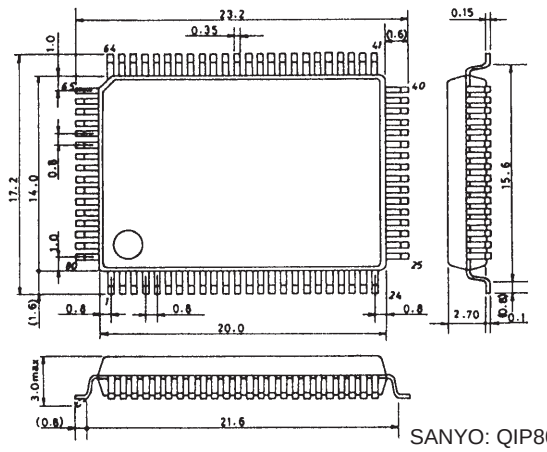
- High-speed programmable divider
- Program memory (ROM)
  - — LC72336: 6143 × 16 bits (12 kB)
  - — LC72338: 8191 × 16 bits (16 kB)
- Data memory (RAM): 512 × 4 bits
- All instructions are one-word instructions
- Cycle time: 1.33 µs
- Stack: 8 levels
- LCD drivers: Up to 96 segments (1/3 duty, 1/3 bias)
- Serial I/O: Up to 3 channels (8-bit 3-wire type)
- External interrupts: 2 interrupts (INT0, INT1)
  Interrupt on rising or falling edge (selectable)
- Internal interrupts: 3 interrupt
  Two built-in timer interrupts and 1 serial I/O interrupt
- Nested interrupt levels: 4 levels
- D/A converter: 4 channels (8-bit PWM output)
- A/D converter: 4 channels
  (6-bit successive approximation)
- General-purpose ports:
  - — Input ports: 8
  - — Output ports: 12 (16 maximum)
  - — I/O ports: 8 (20 maximum, can be switched between input and output in bit units.)
- PLL block: Supports 4 types of dead zone control, and includes a built-in unlock detection circuit.
  Supports 12 different reference frequencies.
- Universal counter: 20 bits (Can be used for either frequency or period measurement.)
- Timers: Eight types of time measurement
- Beep function: Six beep tones
- Reset: Built-in voltage detection type reset circuit
- Halt mode: Stops the controller operating clock.
- Operating supply voltage: 4.5 to 5.5 V (3.5 to 5.5 V if only the controller block operates.)

Package Dimensions

unit: mm

3174-QFP80E

[LC72336, 72338]



SANYO: QIP80E

This LSI can easily use CCB that is SANYO's original bus format.

- **CCB is a trademark of SANYO ELECTRIC CO., LTD.**
- **CCB is SANYO's original bus format and all the bus addresses are controlled by SANYO.**

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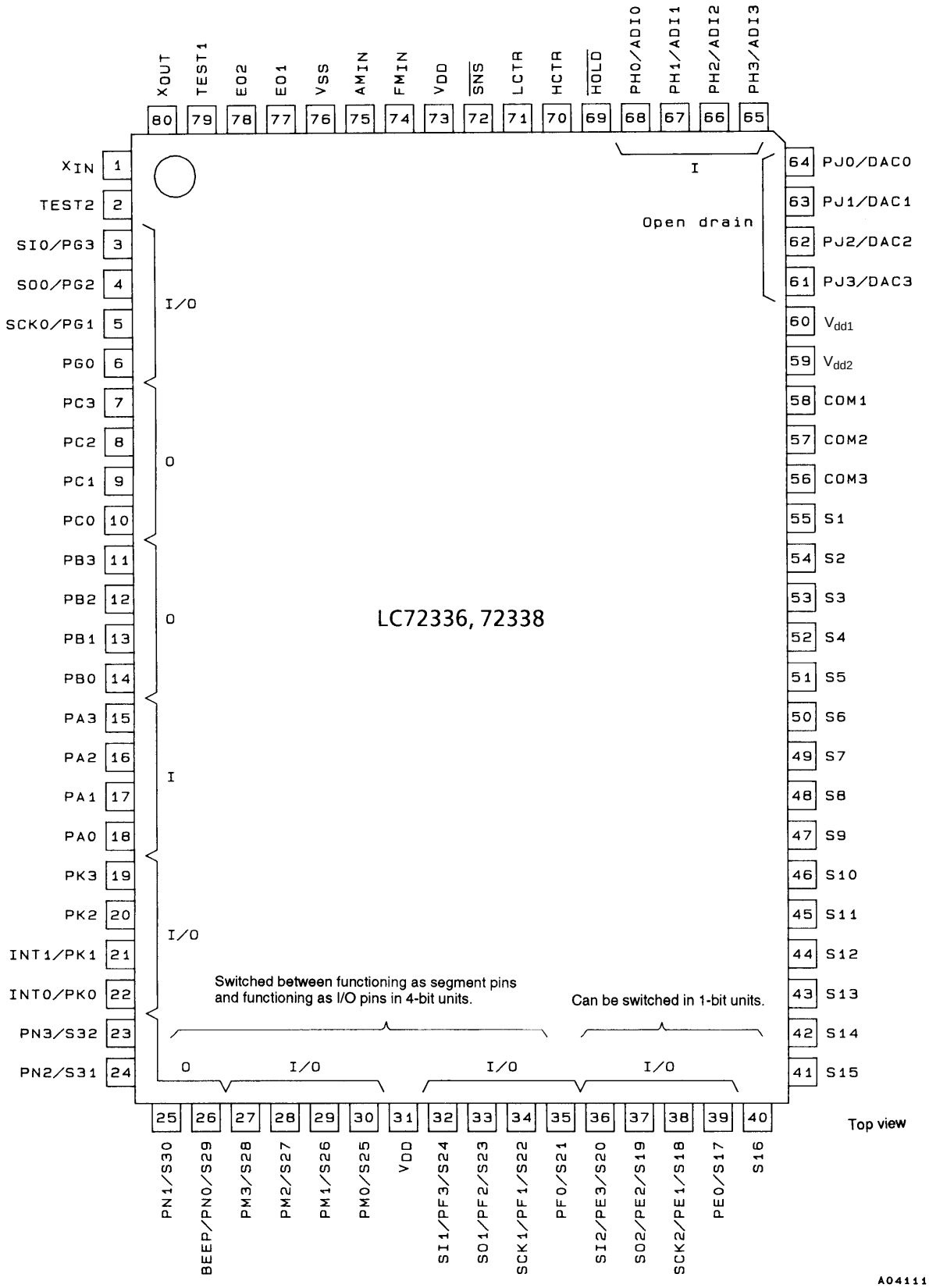
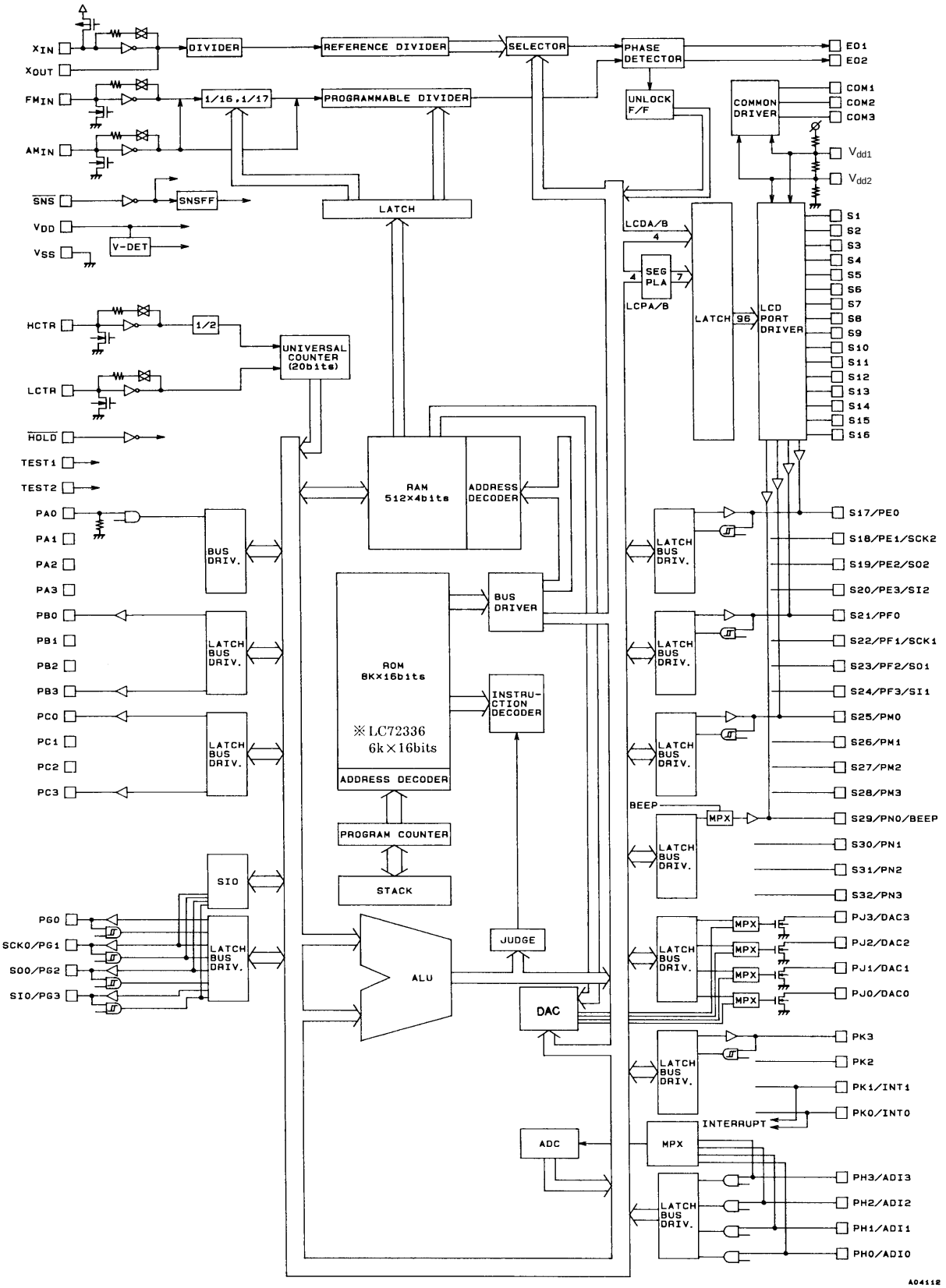
Pin Assignment



Block Diagram



Specifications

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max		–0.3 to +6.5	V
Input voltage	V_{IN}	All input pins	–0.3 to V_{DD} + 0.3	V
Output voltage	V_{OUT} (1)	Port PJ	–0.3 to +15	V
	V_{OUT} (2)	All output ports other than V_{OUT} (1)	–0.3 to V_{DD} + 0.3	V
Output current	I_{OUT} (1)	Port PJ	0 to +5	mA
	I_{OUT} (2)	PE, PF, PG, PK, PM, PN, EO1, EO2	0 to +3	mA
	I_{OUT} (3)	Ports PB and PC	0 to +1	mA
	I_{OUT} (4)	S1 to S32	300	µA
	I_{OUT} (5)	COM1 to COM3	3	mA
Allowable power dissipation	Pd max	Ta = –45 to 85°C	300	mW*
Operating temperature	Topr		–40 to +85	°C
Storage temperature	Tstg		–45 to +125	°C

Note: * Reference value

Allowable Operating Ranges at Ta = –40 to +85°C, V_{DD} = 3.5 to 5.5 V

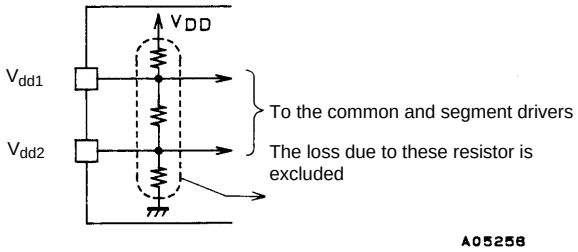
Parameter	Symbol	Conditions	min	typ	max	Unit
Supply voltage	V_{DD} (1)	CPU and PLL operating	4.5	5.0	5.5	V
	V_{DD} (2)	CPU operating	3.5		5.5	V
	V_{DD} (3)	Memory retention	1.3		5.5	V
Input high-level voltage	V_{IH} (1)	Ports PE, PH, and PM, HCTR and LCTR (when selected for input)	0.7 V_{DD}		V_{DD}	V
	V_{IH} (2)	Ports PF, PG, and PK, LCTR (frequency measurement mode), and $\overline{HOLD}$	0.8 V_{DD}		V_{DD}	V
	V_{IH} (3)	$\overline{SNS}$	2.5		V_{DD}	V
	V_{IH} (4)	Port PA	0.6 V_{DD}		V_{DD}	V
Input low-level voltage	V_{IL} (1)	Port PE, PH, and PM, HCTR and LCTR (when selected for input)	0		0.3 V_{DD}	V
	V_{IL} (2)	Port PA, PF, PG, and PK, LCTR (frequency measurement mode)	0		0.2 V_{DD}	V
	V_{IL} (3)	$\overline{SNS}$	0		+1.3	V
	V_{IL} (4)	$\overline{HOLD}$	0		0.4 V_{DD}	V
Input frequency	f_{IN} (1)	XIN	4.0	4.5	5.0	MHz
	f_{IN} (2)	FMIN: V_{IN} (2), V_{DD} (1)	10		150	MHz
	f_{IN} (3)	FMIN: V_{IN} (3), V_{DD} (1)	10		130	MHz
	f_{IN} (4)	AMIN (H): V_{IN} (3), V_{DD} (1)	2.0		40	MHz
	f_{IN} (5)	AMIN (L): V_{IN} (3), V_{DD} (1)	0.5		10	MHz
	f_{IN} (6)	HCTR: V_{IN} (3), V_{DD} (1)	0.4		12	MHz
	f_{IN} (7)	LCTR: V_{IN} (3), V_{DD} (1)	100		500	kHz
	f_{IN} (8)	LCTR (frequency measurement mode): V_{IH} (2), V_{IL} (2), V_{DD} (1)	1		20×10^3	Hz
Input amplitude	V_{IN} (1)	XIN	0.5		1.5	Vrms
	V_{IN} (2)	FMIN	0.10		1.5	Vrms
	V_{IN} (3)	FMIN, AMIN, HCTR, LCTR	0.07		1.5	Vrms
Input voltage range	V_{IN} (4)	ADI0 to ADI3	0		V_{DD}	V

Electrical Characteristics for the Allowable Operating Ranges

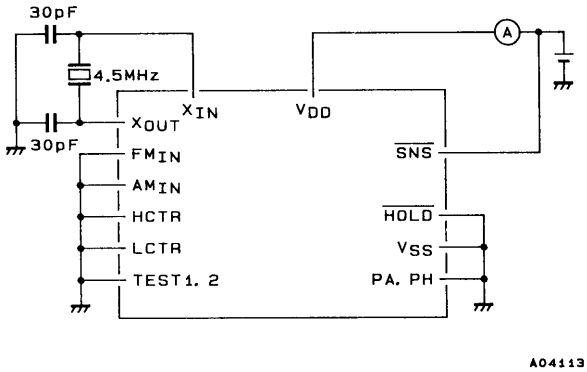
Parameter	Symbol	Conditions	min	typ	max	Unit
Input high-level current	I_{IH} (1)	XIN: $V_I = V_{DD} = 5.0$ V	2.0	5.0	15	µA
	I_{IH} (2)	FMIN, AMIN, HCTR, LCTR: $V_I = V_{DD} = 5.0$ V	4.0	10	30	µA
	I_{IH} (3)	Ports PA, PE, PF, PG, PH, PK, and PM, $\overline{SNS}$, $\overline{HOLD}$, HCTR, LCTR: No pull-down resistors on port PA, $V_I = V_{DD} = 5.0$ V, with input mode selected for ports PE, PF, PG, PK, and PM			3.0	µA
	I_{IH} (4)	With pull-down resistors on port PA, $V_I = V_{DD} = 5.0$ V		50		µA
Input low-level current	I_{IL} (1)	XIN: $V_I = V_{SS}$	2.0	5.0	15	µA
	I_{IL} (2)	FMIN, AMIN, HCTR, LCTR: $V_I = V_{SS}$	4.0	10	30	µA
	I_{IL} (3)	Ports PA, PE, PF, PG, PH, PK, and PM, $\overline{SNS}$, $\overline{HOLD}$, HCTR, LCTR: No pull-down resistors on port PA, $V_I = V_{SS}$, with input mode selected for ports PE, PF, PG, PK, and PM			3.0	µA
Input floating voltage	V_{IF}	With pull-down resistors on port PA			0.05 V_{DD}	V
Pull-down resistance	R_{PD} (1)	With pull-down resistors on port PA, $V_{DD} = 5$ V	75	100	200	kΩ
Hysteresis	V_H	Ports PF, PG, and PK, LCTR (in frequency measurement mode)	0.1 V_{DD}	0.2 V_{DD}		V
Output high-level voltage	V_{OH} (1)	Ports PB and PC: $I_O = -1$ mA	$V_{DD} - 2.0$			V
	V_{OH} (2)	Ports PE, PF, PG, PK, PM, and PN: $I_O = -1$ mA	$V_{DD} - 1.0$			V
	V_{OH} (3)	EO1, EO2: $I_O = -500$ µA	$V_{DD} - 1.0$			V
	V_{OH} (4)	XOUT: $I_O = -200$ µA	$V_{DD} - 1.0$			V
	V_{OH} (5)	S1 to S32: $I_O = -20$ µA	$V_{DD} - 1.0$			V
	V_{OH} (6)	COM1, COM2, COM3: $I_O = -100$ µA	$V_{DD} - 1.0$			V
Output low-level voltage	V_{OL} (1)	Ports PB and PC: $I_O = 50$ µA			2.0	V
	V_{OL} (2)	Ports PE, PF, PG, PK, PM, and PN: $I_O = 1$ mA			1.0	V
	V_{OL} (3)	EO1, EO2: $I_O = 500$ µA			1.0	V
	V_{OL} (4)	XOUT: $I_O = 200$ µA			1.0	V
	V_{OL} (5)	S1 to S32: $I_O = 20$ µA			1.0	V
	V_{OL} (6)	COM1, COM2, COM3: $I_O = 100$ µA			1.0	V
	V_{OL} (7)	Port PJ: $I_O = 5$ mA	0.75		2.0	V
Output mid-level voltage	V_{MID} (1)	S1 to S32: $I_O = \pm 20$ µA	2/3 $V_{DD} \pm$ 1.0			V
	V_{MID} (2)	S1 to S32: $I_O = \pm 20$ µA	1/3 $V_{DD} \pm$ 1.0			V
	V_{MID} (3)	COM1, COM2, COM3: $I_O = \pm 100$ µA	2/3 $V_{DD} \pm$ 1.0			V
	V_{MID} (4)	COM1, COM2, COM3: $I_O = \pm 100$ µA	1/3 $V_{DD} \pm$ 1.0			V
Output off leakage current	I_{OFF} (1)	Ports PE, PF, PG, PK, PM, and PN	–3.0		+3.0	µA
	I_{OFF} (2)	EO1 , EO2	–100		+100	nA
	I_{OFF} (3)	Port PJ	–5.0		+5.0	µA
AD conversion error	—	ADI0 to ADI3: V_{DD} (1)	–1/2		+1/2	LSB
Reject pulse width	P_{REJ}	$\overline{SNS}$			50	µs
Power-down detection voltage	V_{DET}		2.7	3.0	3.3	V
Pull-down resistance	R_{PD} (2)	TEST1, TEST2		10		kΩ
Current drain	I_{DD} (1)	V_{DD} (1): f_{IN} (2) = 130 MHz, Ta = 25°C		12		mA
	I_{DD} (2)	V_{DD} (2): halt mode*, Ta = 25°C (Fig. 1)		0.45		mA
	I_{DD} (3)	$V_{DD} = 5.5$ V, oscillator stopped, Ta = 25°C (Fig. 2)			5	µA
	I_{DD} (4)	$V_{DD} = 2.5$ V, oscillator stopped, Ta = 25°C (Fig. 2)			1	µA

Note: * In case of instruction execution for 20 steps at intervals of 1 ms, with the PLL, counter functions and other functions all stopped.

Note: 1. Except for the divider resistors used for the bias voltage generation circuit incorporated in the V_{dd1} and V_{dd2} systems.

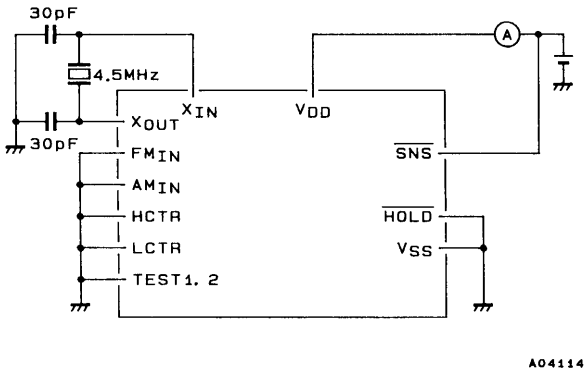


Test Circuits



Note: With all ports other than those indicated in the figure open.
With the segment port function selected for ports PE, PF, PM, and PN.
With the output function selected for ports PG and PK.

Figure 1 $I_{DD}2$, $I_{DD}3$, and $I_{DD}4$ in Hold Mode



Note: With all ports other than those indicated in the figure open.
With the segment port function selected for ports PE, PF, PM, and PN.
With the output function selected for ports PG and PK.

Figure 2 $I_{DD}5$ in Backup Mode

Pin Functions

Pin No.	Symbol	I/O	I/O type	Function
18 17 16 15	PA0 PA1 PA2 PA3	I	Inputs with pull-down resistors	These are special-purpose ports for key return signal inputs. Their threshold voltage is set lower than that of other inputs. When a key matrix is formed in conjunction with ports PB and PC, up to three simultaneous key presses can be detected. The pull-down resistors are set up for all four pins by the IOS instruction (Pn = 2, b1). This cannot be specified on an individual pin basis. Input is disabled in clock stop mode.
14 13 12 11 10 9 8 7	PB0 PB1 PB2 PB3 PC0 PC1 PC2 PC3	O	Unbalanced CMOS push-pull circuits	These are special-purpose ports for key return signal outputs. No diodes for preventing short-circuits due to multiple simultaneous key presses are required since the output transistor circuits are unbalanced CMOS circuits. These pins become high-impedance outputs in clock stop mode. These pins function as high-impedance outputs after a power-on reset and retain that state until an output instruction is executed.

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<table>
<tr><th>Pin No.</th><th>Symbol</th><th>I/O</th><th>I/O type</th><th>Function</th></tr>
<tr><td>6
5
4
3</td><td>PG0
PG1/SCK0
PG2/SO0
PG3/SI0</td><td>I/O</td><td>CMOS push-pull</td><td>Shared-function general-purpose output and serial I/O port
Inputs are a Schmitt input.
The IOS instruction is used to switch between the general-purpose I/O port function and the serial I/O function, as well as between input and output for the general-purpose I/O port function.
• When used as a general-purpose I/O port:
Input or output can be specified in bit units (bit I/O).
These ports are set up to be general-purpose I/O ports with the IOS instruction with Pn = 0.
b0 = SI/O0 0 ... General-purpose ports
1 ... SI/O ports
The IOS instruction is used to specify input or output in bit units.
PG ... Pn = 6 0 ... Input
1 ... Output
• When used as a serial I/O port:
These ports are set up to be serial I/O ports with the IOS instruction with Pn = 0.
The contents of the serial I/O data buffers can be saved and loaded with the INR and OUTR instructions.
Note: Pin setup states when used as serial I/O ports:
PG0 ... General-purpose I/O
PG1 ... SCK0 output in internal clock mode
SCK0 input in external clock mode
PG2 ... SO0 output
PG3 ... SI0 input
These ports go to the input disabled high-impedance state in clock stop mode.
These ports function as general-purpose input ports after a power-on reset.</td></tr>
<tr><td>1
80</td><td>XIN
XOUT</td><td>I
O</td><td>—</td><td>4.5 MHz crystal oscillator connections</td></tr>
<tr><td>77
78</td><td>EO1
EO2</td><td>O</td><td>CMOS tristate</td><td>Charge pump outputs
These pins go to the high-impedance state when the $\overline{\text{HOLD}}$ pin is set low in the hold enable state.
These pins go to the high-impedance state in clock stop mode, after a power-on reset, and in the PLL stopped state.</td></tr>
<tr><td>76
31, 73</td><td>V_{SS}
V_{DD}</td><td>—</td><td>—</td><td>Power supply connections</td></tr>
<tr><td>75</td><td>AMIN</td><td>I</td><td>CMOS amplifier input</td><td>AM VCO (local oscillator) input
This pin is selected and the band set using the PLL instruction CW1 (b1 and b0) field.
<table><tr><th>b1</th><th>b0</th><th>Band</th></tr><tr><td>1</td><td>0</td><td>2 to 40 MHz (SW)</td></tr><tr><td>1</td><td>1</td><td>0.5 to 10 MHz (MW, LW)</td></tr></table>
The input signal must be capacitor coupled.
Input is disabled if the $\overline{\text{HOLD}}$ pin is set low in the HOLD enabled state.
Input is disabled in clock stop mode, after a power-on reset, and in the PLL stopped state.</td></tr>
<tr><td>74</td><td>FMIN</td><td>I</td><td>CMOS amplifier input</td><td>FM VCO (local oscillator) input
This pin is selected using the PLL instruction CW1 field (b1 = 0, b0 = don’t care).
The input signal must be capacitor coupled.
Input is disabled if the $\overline{\text{HOLD}}$ pin is set low in the HOLD enabled state.
Input is disabled in clock stop mode, after a power-on reset, and in the PLL stopped state.</td></tr>
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Pin No.	Symbol	I/O	I/O type	Function
72	$\overline{SNS}$	I	CMOS input	Shared-function voltage sensing input and general-purpose input port The input threshold voltage is set lower than that of other inputs. • When used as a voltage sensing pin: This pin is used to recognize power failures on recovery from backup (clock stop) mode. An internal sensing flip-flop is used for this determination. The TUL instruction (b2) can be used to test the sense flip-flop. • When used as a general-purpose input port: Use the TUL instruction (b3) to test this pin when it is used as a general-purpose input port. Unlike other input ports, input is not disabled during clock stop mode or a power-on reset. Thus applications must take through currents into consideration if this pin is used as a general-purpose input port.
71	LCTR	I	CMOS amplifier input	Shared-function universal counter (frequency or period measurement) and general-purpose input port The IOS instruction (Pn = 3, b3) is used to switch this pin between its universal counter and general-purpose input port functions. • When used for frequency measurement: Select the universal counter function with an IOS instruction (Pn = 3, b3 = 0). Set LCTR frequency measurement mode with a UCS instruction (b3 = 0, b2 = 1). After selecting the measurement time, start the counter with a UCC instruction. The CNTEND flag will be set when the count completes. Since this circuit operates as an AC amplifier in this mode, the input must be capacitor coupled. • When used for period measurement: With the universal counter function selected, set period measurement mode with a UCS instruction (b3 = 1, b2 = 0). After selecting the measurement time, start the counter with a UCC instruction. The CNTEND flag will be set when the count completes. Since the bias feedback resistor is switched off in this mode, the input must be DC coupled. • When used as a general-purpose input port: Specify the general-purpose input port function with an IOS instruction (Pn = 3, b3 = 1). Use the INR (b1) internal register (address 0EH) input instruction to read in the input data. Input is disabled in clock stop mode. (The input pin is pulled down.) The universal counter function is selected after a power-on reset. (HCTR frequency measurement mode.)

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Pin No.	Symbol	I/O	I/O type	Function
70	HCTR	I	CMOS amplifier input	Shared-function universal counter input and general-purpose input port The IOS instruction (Pn = 3, b3) is used to switch this pin between its universal counter and general-purpose input port functions. • When used for frequency measurement: Select the universal counter function with an IOS instruction (Pn = 3, b2 = 0). Set HCTR frequency measurement mode with a UCS instruction (b3 = 0, b2 = 0). After selecting the measurement time, start the counter with a UCC instruction. The CNTEND flag will be set when the count completes. Since this circuit operates as an AC amplifier in this mode, the input must be capacitor coupled. • When used as a general-purpose input port: Set the general-purpose input port function with an IOS instruction (Pn = 3, b2 = 1). Use the INR (b1) internal register (address 0EH) input instruction to read in the input data. Input is disabled in clock stop mode. (The input pin is pulled down.) The universal counter function is selected after a power-on reset.
69	$\overline{\text{HOLD}}$	I	CMOS input	Controls the PLL circuit and clock stop mode. When this pin is set low in the hold enabled state, FMIN and AMIN pin input is disabled and the EO pin goes to the high-impedance state. To switch to clock stop mode, set the HOLDEN flag, set this pin low, and execute a CKSTP instruction. Set this pin high to clear clock stop mode.
68 67 66 65	PH0/ADI0 PH1/ADI1 PH2/ADI2 PH3/ADI3	I	CMOS input Analog input	Shared-function general-purpose input and A/D converter input port The IOS instruction (Pn = 7) is used to switch these pins between the general-purpose and A/D converter input port functions. • When used as a general-purpose input port: Set the general-purpose input port function (in bit units) with the IOS instruction (Pn = 7). • When used for A/D converter input: Set the A/D converter input port function with an IOS instruction (Pn = 7). Specify the pin to convert with an IOS instruction (Pn = 1). Start the conversion with a UCC instruction (b2). The ADCE flag is set when the conversion has completed. Note: Since input is disabled, low will always be returned if an input instruction (the IN instruction) is executed for a port specified for A/D converter input. (In other words, the port must be set to the general-purpose input function before the input instruction is executed.) Input is disabled in clock stop mode. The general-purpose input function is selected after a power-on reset.

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Pin No.	Symbol	I/O	I/O type	Function
64 63 62 61	PJ0/DAC0 PJ1/DAC1 PJ2/DAC2 PJ3/DAC3	O	N-channel open drain	Shared-function general-purpose and D/A converter output port The IOS instruction (Pn = 9) is used to switch these pins between the general-purpose and D/A converter output port functions. Since these pins are open drain circuits, pull-up resistors are required in external circuits accepting these outputs. • When used as a general-purpose port: Set the general-purpose input port function with the IOS instruction (Pn = 9). • When used for D/A converter output: Use the IOS instruction (Pn = 9) to switch the port in bit units. D/A converter data is loaded into the DAC0 to DAC3 specified with the DAC instruction. Although a PWM waveform is output as soon as the port is switched, after data is loaded, the data prior to that load is output for up to 114 µs (1/8.79 kHz). In clock stop mode, these outputs go to the transistor off (high output) state. The general-purpose output port function is selected after a power-on reset, and the outputs go to the transistor off (high output) state.
22 21 20 19	PK0/INT0 PK1/INT1 PK2 PK3	I/O	CMOS push-pull	Shared-function general-purpose I/O and external interrupt port There is no instruction that switches between the general-purpose port and the external interrupt pin functions. Rather, the corresponding pin becomes an input-only pin (output disabled) at the point where the external interrupt enable flag for that pin is set. • When used as a general-purpose I/O port: Input or output can be specified in bit units (bit I/O). The IOS instruction is used to specify input or output in bit units. • When used as external interrupt pins: These pins are enabled by setting the external interrupt enable flags (INT0EN and INT1EN) in status register 2. At that point the pin is automatically set up to be an input port. The status register 1 interrupt enable flag (INTEN) must also be set to enable interrupt operation. Use the IOS instruction (Pn = 3, b1 = INT1, b0 = INT0) to select rising or falling edge detection. Input is disabled with the pins in the high-impedance state in clock stop mode. The general-purpose input port function is selected after a power-on reset.
60	Vdd1		—	Apply the LCD drive bias 2/3 voltage to this pin.
59	Vdd2		—	Apply the LCD drive bias 1/3 voltage to this pin.
79 2	TEST1 TEST2		—	LSI test pin This pin must be left open or connected to ground.
58 57 56	COM1 COM2 COM3	O	CMOS 3-value output	LCD driver common output pins This drive circuit implements a 1/3-duty, 1/3-bias drive scheme. These pins are fixed at the low level in clock stop mode. These pins are fixed at the low level after a power-on reset.
55 to 40	S1 to S16	O	CMOS 3-value output	LCD driver segment output pins This drive circuit implements a 1/3-duty, 1/3-bias drive scheme. The frame frequency is 100 Hz. These pins are fixed at the low level in clock stop mode. These pins are fixed at the low level after a power-on reset.

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Pin No.	Symbol	I/O	I/O type	Function
39 38 37 36	S17/PE0 S18/PE1/SCK2 S19/PE2/SO2 S20/PE3/SI2	I/O	CMOS 3-value output and push-pull	Shared-function LCD driver segment output, general-purpose I/O, and serial I/O port The IOS instruction is used to switch between the LCD driver segment output, general-purpose I/O, and serial I/O functions, and to switch between input and output for the general-purpose input port function. • When used for segment output: The function can be specified in bit units. Segment output is specified with the IOS instruction (Pn = 0DH). b0 = S17/PE0 0 ... Segment output b1 = S18/PE1 1 ... PE0 to PE3 output b2 = S19/PE2 b3 = S20/PE3 • When used as a general-purpose I/O port: Input or output can be specified in bit units (1-bit I/O). The general-purpose I/O port function is specified with the IOS instruction (Pn = 0). b2 = SI/O2 0 ... General-purpose port 1 ... SI/O port Input or output is specified with the IOS instruction in bit units. PE ... Pn = 4 0 ... Input 1 ... Output • When used as a serial I/O port: The serial I/O port function is specified with the IOS instruction (Pn = 0). The contents of the serial I/O data buffer can be saved and loaded with the INR and OUTR instructions. Note: Pin setup states when used as a serial I/O port: PE0 ... General-purpose I/O PE1 ... SCK2 output in internal clock mode SCK2 input in external clock mode PE2 ... SO2 output PE3 ... SI2 input In clock stop mode, if this port is used as a general-purpose I/O port or as a serial I/O port, the pins go to the input disabled high-impedance state. If used for segment output, the pins are fixed at the low level. The segment output port function is selected after a power-on reset.

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Pin No.	Symbol	I/O	I/O type	Function
35 34 33 32	S21/PF0 S22/PF1/SCK1 S23/PF2/SO1 S24/PF3/SI1	I/O	CMOS 3-value output and push-pull	Shared-function LCD driver segment output, general-purpose I/O, and serial I/O port The PF0 to PF3 inputs are Schmitt inputs. The IOS instruction is used to switch between the LCD driver segment output, general-purpose I/O, and serial I/O functions, and to switch between input and output for the general-purpose input port function. • When used for segment output: The function is specified in 4-bit units. Segment output is specified with the IOS instruction (Pn = 0EH). b0 = S21 to S24/PF0 to PF3 0 ... Segment output 1 ... PF0 to PF3 output • When used as a general-purpose I/O port: Input or output can be specified in bit units (1-bit I/O). The general-purpose I/O port function is specified with the IOS instruction (Pn = 0). b1 = SI/O1 0 ... General-purpose port 1 ... SI/O port Input or output is specified with the IOS instruction in bit units. PF ... Pn = 5 0 ... Input 1 ... Output • When used as a serial I/O port: The serial I/O port function is specified with the IOS instruction (Pn = 0). The contents of the serial I/O data buffer can be saved and loaded with the INR and OUTR instructions. Note: Pin setup states when used as a serial I/O port: PF0 ... General-purpose I/O PF1 ... SCK1 output in internal clock mode SCK1 input in external clock mode PF2 ... SO1 output PF3 ... SI1 input In clock stop mode, if this port is used as a general-purpose I/O port or as a serial I/O port, the pins go to the input disabled high-impedance state. If used for segment output, the pins are fixed at the low level. The segment output port function is selected after a power-on reset.
30 29 28 27	S25/PM0 S26/PM1 S27/PM2 S28/PM3	I/O	CMOS 3-value output and push-pull	Shared-function LCD driver segment output and general-purpose I/O port The IOS instruction is used to switch between the LCD driver segment output and the general-purpose I/O functions, and to switch between input and output for the general-purpose input port function. • When used for segment output: The function is specified in 4-bit units. Segment output is specified with the IOS instruction (Pn = 0EH). b1 = S25 to S28/PM0 to PM3 0 ... Segment output 1 ... PF0 to PF3 output • When used as a general-purpose I/O port: Input or output can be specified in bit units (1-bit I/O). Input or output is specified with the IOS instruction in bit units. PM ... Pn = 0CH 0 ... Input 1 ... Output In clock stop mode, if this port is used as a general-purpose I/O port, the pins go to the input disabled high-impedance state. If used for segment output, the pins are fixed at the low level. The segment output port function is selected after a power-on reset.

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Pin No.	Symbol	I/O	I/O type	Function
26 25 24 23	S29/PN0/BEEP S30/PN1 S31/PN2 S32/PN3	O	CMOS 3-value output and push-pull	Shared-function segment output, general-purpose output, and beep tone output port The IOS instruction is used to switch between the segment output port and the PN0 to PN3 functions. The BEEP instruction is used to switch between the general-purpose output port and the beep tone output functions. • When used for segment output: The function can be specified in 3-bit units. Segment output is specified with the IOS instruction (Pn = 0EH). b2 = S29 to S32/PN0 to PN3 0 ... Segment output 1 ... PN0 to PN3 output • When used as a general-purpose output port: The general-purpose output port function is selected with the BEEP instruction (b3 = 0). PN1 to PN3 are dedicated general-purpose output function pins. • When used as the BEEP output pin: Beep tone output is specified with the BEEP instruction (b3 = 1). The frequency is specified with the BEEP instruction (b0, b1, and b2). When the beep tone function is specified, executing an output instruction will only overwrite the contents of the internal latch. It will have no effect on the output whatsoever. In clock stop mode, if this port is used as a general-purpose output port, the pins go to the input disabled high-impedance state. If used for segment output, the pins are fixed at the low level. The segment output port function is selected after a power-on reset.

LC723336 and LC72338 Instruction Table

Abbreviations:
ADDR: Program memory address
b: Borrow
C: Carry
D_H: Data memory address high (row address) [2 bits]
D_L: Data memory address low (column address) [4 bits]
I: Immediate data [4 bits]
M: Data memory address
N: Bit position [4 bits]
Pn: Port number [4 bits]
r: General register (one of the locations 00 to 0FH in bank)
Rn: Register number [4 bits]
( ): Contents of register or memory
( )N: Contents of bit N of register or memory

Instruction group	Mnemonic	Operand		Function	Operation	Machine code													
		1st	2nd			D15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	D0
Addition instructions	AD	r	M	Add M to r	r ← (r) + (M)	0	1	0	0	0	0	D_H		D_L				r			
	ADS	r	M	Add M to r, then skip if carry	r ← (r) + (M) skip if carry	0	1	0	0	0	1	D_H		D_L				r			
	AC	r	M	Add M to r with carry	r ← (r) + (M) + C	0	1	0	0	1	0	D_H		D_L				r			
	ACS	r	M	Add M to r with carry, then skip if carry	r ← (r) + (M) + C skip if carry	0	1	0	0	1	1	D_H		D_L				r			
	AI	M	I	Add I to M	M ← (M) + I	0	1	0	1	0	0	D_H		D_L				I			
	AIS	M	I	Add I to M, then skip if carry	M ← (M) + I skip if carry	0	1	0	1	0	1	D_H		D_L				I			
	AIC	M	I	Add I to M with carry	M ← (M) + I + C	0	1	0	1	1	0	D_H		D_L				I			
	AICS	M	I	Add I to M with carry, then skip if carry	M ← (M) + I + C skip if carry	0	1	0	1	1	1	D_H		D_L				I			
Subtraction instructions	SU	r	M	Subtract M from r	r ← (r) – (M)	0	1	1	0	0	0	D_H		D_L				r			
	SUS	r	M	Subtract M from r, then skip if borrow	r ← (r) – (M) skip if borrow	0	1	1	0	0	1	D_H		D_L				r			
	SB	r	M	Subtract M from r with borrow	r ← (r) – (M) – b	0	1	1	0	1	0	D_H		D_L				r			
	SBS	r	M	Subtract M from r with borrow, then skip if borrow	r ← (r) – (M) – b skip if borrow	0	1	1	0	1	1	D_H		D_L				r			
	SI	M	I	Subtract I from M	M ← (M) – I	0	1	1	1	0	0	D_H		D_L				I			
	SIS	M	I	Subtract I from M, then skip if borrow	M ← (M) – I skip if borrow	0	1	1	1	0	1	D_H		D_L				I			
	SIB	M	I	Subtract I from M with borrow	M ← (M) – I – b	0	1	1	1	1	0	D_H		D_L				I			
	SIBS	M	I	Subtract I from M with borrow, then skip if borrow	M ← (M) – I – b skip if borrow	0	1	1	1	1	1	D_H		D_L				I			
Comparison instructions	SEQ	r	M	Skip if r equal to M	(r) – (M) skip if zero	0	0	0	1	0	0	D_H		D_L				r			
	SEQI	M	I	Skip if M equal to I	(M) – I skip if zero	0	0	0	1	0	1	D_H		D_L				I			
	SNEI	M	I	Skip if r not equal to M	(M) – I skip if not zero	0	0	0	0	0	1	D_H		D_L				I			
	SGE	r	M	Skip if r is greater than or equal to M	(r) – (M) skip if not borrow	0	0	0	1	1	0	D_H		D_L				r			
	SGEI	M	I	Skip if M is greater than or equal to I	(M) – I skip if not borrow	0	0	0	1	1	1	D_H		D_L				I			
	SLEI	M	I	Skip if M is less than I	(M) – I skip if borrow	0	0	0	0	1	1	D_H		D_L				I			

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Instruction group	Mnemonic	Operand 1st	Operand 2nd	Function	Operation	Machine code D15 14 13 12	11 10	9 8	7 6 5 4	3 2 1 D0
Logical operation instructions	AND	r	M	AND M with r	r ← (r) AND (M)	0 0 1 0	0 0	D_H	D_L	r
	ANDI	M	I	AND I with M	M ← (M) AND I	0 0 1 0	0 1	D_H	D_L	I
	OR	r	M	OR M with r	r ← (r) OR (M)	0 0 1 0	1 0	D_H	D_L	r
	ORI	M	I	OR I with M	M ← (M) OR I	0 0 1 0	1 1	D_H	D_L	I
	EXL	r	M	Exclusive OR M with r	r ← (r) XOR (M)	0 0 1 1	0 0	D_H	D_L	r
	EXLI	M	I	Exclusive OR I with M	M ← (M) XOR I	0 0 1 1	0 1	D_H	D_L	I
Transfer instructions	LD	r	M	Load M to r	r ← (M)	1 1 0 1	0 0	D_H	D_L	r
	ST	M	r	Store r to M	M ← (r)	1 1 0 1	0 1	D_H	D_L	r
	MVRD	r	M	Move M to destination M referring to r in the same row	[D_H, Rn] ← (M)	1 1 0 1	1 0	D_H	D_L	r
	MVRS	M	r	Move source M referring to r to M in the same row	M ← [D_H, Rn]	1 1 0 1	1 1	D_H	D_L	r
	MVSR	M1	M2	Move M to M in the same row	[D_H, D_L1] ← [D_H, D_L2]	1 1 1 0	0 0	D_H	D_L1	D_L2
	MVI	M	I	Move I to M	M ← I	1 1 1 0	0 1	D_H	D_L	I
Bit test instructions	TMT	M	N	Test M bits, then skip if all bits specified are true	if M (N) = all “1”, then skip	1 1 1 1	0 0	D_H	D_L	N
	TMF	M	N	Test M bits, then skip if all bits specified are false	if M (N) = all “0”, then skip	1 1 1 1	0 1	D_H	D_L	N
Jump and subroutine call instructions	JMP	ADDR		Jump to the address	PC ← ADDR	1 0 0	ADDR (13 bits)			
	CAL	ADDR		Call subroutine	Stack ← (PC) + 1	1 0 1	ADDR (13 bits)			
	RT			Return from subroutine	PC ← Stack	0 0 0 0	0 0 0 0		1 0 0 0	
	RTS			Return from subroutine and skip	PC ← Stack + 1	0 0 0 0	0 0 0 0		1 0 1 0	
	RTB			Return from subroutine with bank data	PC ← Stack BANK ← Stack	1 1 1 1	1 1 1 1		1 1 0 0	
	RTBS			Return from subroutine with bank data and skip	PC ← Stack + 1 BANK ← Stack	1 1 1 1	1 1 1 1		1 1 0 1	
	RTI			Return from interrupt	PC ← Stack BANK ← Stack CARRY ← Stack	0 0 0 0	0 0 0 0		1 0 0 1	
Status register instructions	SS	I	N	Set status register	(Status reg I) N ← 1	1 1 1 1	1 1 1 1		0 0 0	I N
	RS	I	N	Reset status register	(Status reg I) N ← 0	1 1 1 1	1 1 1 1		0 0 1	I N
	TST	I	N	Test status register true	if (Status reg I) N = all “1”, then skip	1 1 1 1	1 1 1 1		0 1	I N
	TSF	I	N	Test status register false	if (Status reg I) N = all “0”, then skip	1 1 1 1	1 1 1 1		1 0	I N
F/F test instruction	TUL	N		Test unlock F/F then skip if it has not been set	if Unlock F/F (N) = all “0”, then skip	0 0 0 0	0 0 0 0		1 1 0 1	N
Internal register transfer instructions	PLL	M	r	Load M to PLL registers	PLL reg ← PLL data	1 1 1 1	1 0	D_H	D_L	r
	DAC	I			DAC reg ← DAC data	0 0 0 0	0 0 0 0	0 0 1 1		I
	INR	M	Rn	Input register/port data to M	M ← (Rn reg)	0 0 1 1	1 0	D_H	D_L	Rn
	OUTR	M	Rn	Output contents of M to register/port	Rn reg ← (M)	0 0 1 1	1 1	DH	DL	Rn

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Instruction group	Mnemonic	Operand 1st	Operand 2nd	Function	Operation	Machine code D15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 D0
Hardware control instructions	SIO	I1	I2	Serial I/O control	SIO ← I1, I2	0 0 0 0	0 0 0 1	I1	I2
	UCS	I		Set I to UCCW1	UCCW1 ← I	0 0 0 0	0 0 0 0	0 0 0 1	I
	UCC	I		Set I to UCCW2	UCCW2 ← I	0 0 0 0	0 0 0 0	0 0 1 0	I
	BEEP	I		Beep control	BEEP reg ← I	0 0 0 0	0 0 0 0	0 1 1 0	I
	DZC	I		Dead zone control	DZC reg ← I	0 0 0 0	0 0 0 0	1 0 1 1	I
	IOS	Pn	I	Set port control word	IOS reg Pn ← I	1 1 1 1	1 1 1 0	Pn	I
	TMS	I			Timmer reg I	0 0 0 0	0 0 0 0	1 1 0 0	I
Bank switching instruction	BANK	I		Select bank	BANK ← I	0 0 0 0	0 0 0 0	0 1 1 1	I
LCD control instructions	LCDA	M	I	Output segment pattern to LCD digit direct	LCD (DIGIT) ← M	1 1 0 0	0 0 D_H	D_L	DIGIT
	LCDB	M	I			1 1 0 0	0 1 D_H	D_L	DIGIT
	LCPA	M	I	Output segment pattern to LCD digit through Logic Array	LCD (DIGIT) ← Logic Array ← M	1 1 0 0	1 0 D_H	D_L	DIGIT
	LCPB	M	I			1 1 0 0	1 1 D_H	D_L	DIGIT
I/O instructions	IN	M	Pn	Input port data to M	M ← (Pn)	1 1 1 0	1 0 D_H	D_L	Pn
	OUT	M	Pn	Output contents of M to port	Pn ← M	1 1 1 0	1 1 D_H	D_L	Pn
	SPB	Pn	N	Set port bits	(Pn) N ← 1	0 0 0 0	0 0 1 0	Pn	N
	RPB	Pn	N	Reset port bits	(Pn) N ← 0	0 0 0 0	0 0 1 1	Pn	N
	TPT	Pn	N	Test port bits, then skip if all bits specified are true	if (Pn) N = all “1”, then skip	1 1 1 1	1 1 0 0	Pn	N
	TPF	Pn	N	Test port bits, then skip if all bits specified are false	if (Pn) N = all “0”, then skip	1 1 1 1	1 1 0 1	Pn	N
Other instructions	HALT	I		Halt mode control	HALT reg ← I, then CPU clock stop	0 0 0 0	0 0 0 0	0 1 0 0	I
	CKSTP			Clock stop	Stop X’tal OSC if HOLD = 0	0 0 0 0	0 0 0 0	0 1 0 1	
	SHR	r			Shift r right with carry	0 0 0 0	0 0 0 0	1 1 1 0	r
	NOP			No operation	No operation	0 0 0 0	0 0 0 0	0 0 0 0	