



# LC72322R, 72323R

## Single-Chip Microcontroller with PLL and LCD Driver

### Overview

The LC72322R and LC72323R are single-chip microcontrollers for use in electronic tuning applications. These ICs include on chip both LCD drivers and a PLL circuit that can operate at up to 150 MHz. The LC72322R and LC72323R feature that these ICs are reversed pin-assignment versions of LC72322 and LC72323 respectively and have the equal functions and specifications to theirs respectively.

### Functions

- Stack: Eight levels
- Fast programmable divider
- General-purpose counters: HCTR for frequency measurement and LCTR for frequency or period measurement
- LCD driver for displays with up to 56 segments (1/2 duty, 1/2 bias)
- Program memory (ROM): 4095 (8 KB) 16-bit digits:  
LC72322R  
3071 (6 KB) 16-bit digits:  
LC72323R
- Data memory (RAM): 256 4-bit digits
- All instructions are single-word instructions
- Cycle time: 2.67  $\mu$ s, 13.33  $\mu$ s, or 40.00  $\mu$ s (option)
- Unlock FF: 0.55  $\mu$ s detection, 1.1  $\mu$ s detection
- Timer FF: 1 ms, 5ms, 25ms, 125ms
- Input ports\*: One dedicated key input port and one high-breakdown voltage port
- Output ports\*: Two dedicated key output ports, one high-breakdown voltage open-drain port

Two CMOS output ports (of which one can be switched to be used as LCD driver outputs)

Seven CMOS output ports (mask option switchable to use as LCD ports)

- I/O ports\*: One switchable between input and output in four-bit units and one switchable between input and output in bit units

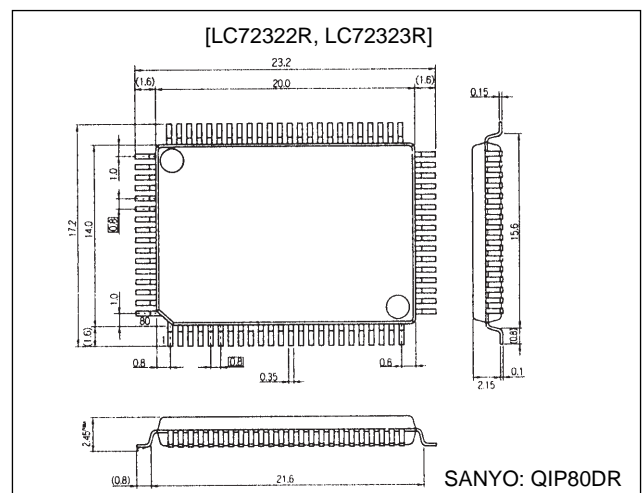
Note: \* Each port consists of four bits.

- Program runaway can be detected and a special address set (Programmable watchdog timer).
- Voltage detection type reset circuit
- One 6-bit A/D converter
- Two 8-bit D/A converters (PWM): LC72322R only
- One external interrupt
- Hold mode for RAM backup
- Sense FF for hot/cold startup determination
- PLL: 4.5 to 5.5 V
- CPU: 3.5 to 5.5 V
- RAM: 1.3 to 5.5 V
- LC72P321R as OTP used
- Package: QIP80DR

### Package Dimensions

unit: mm

#### 3223-QFP80DR



This LSI can easily use CCB that is SANYO's original bus format.



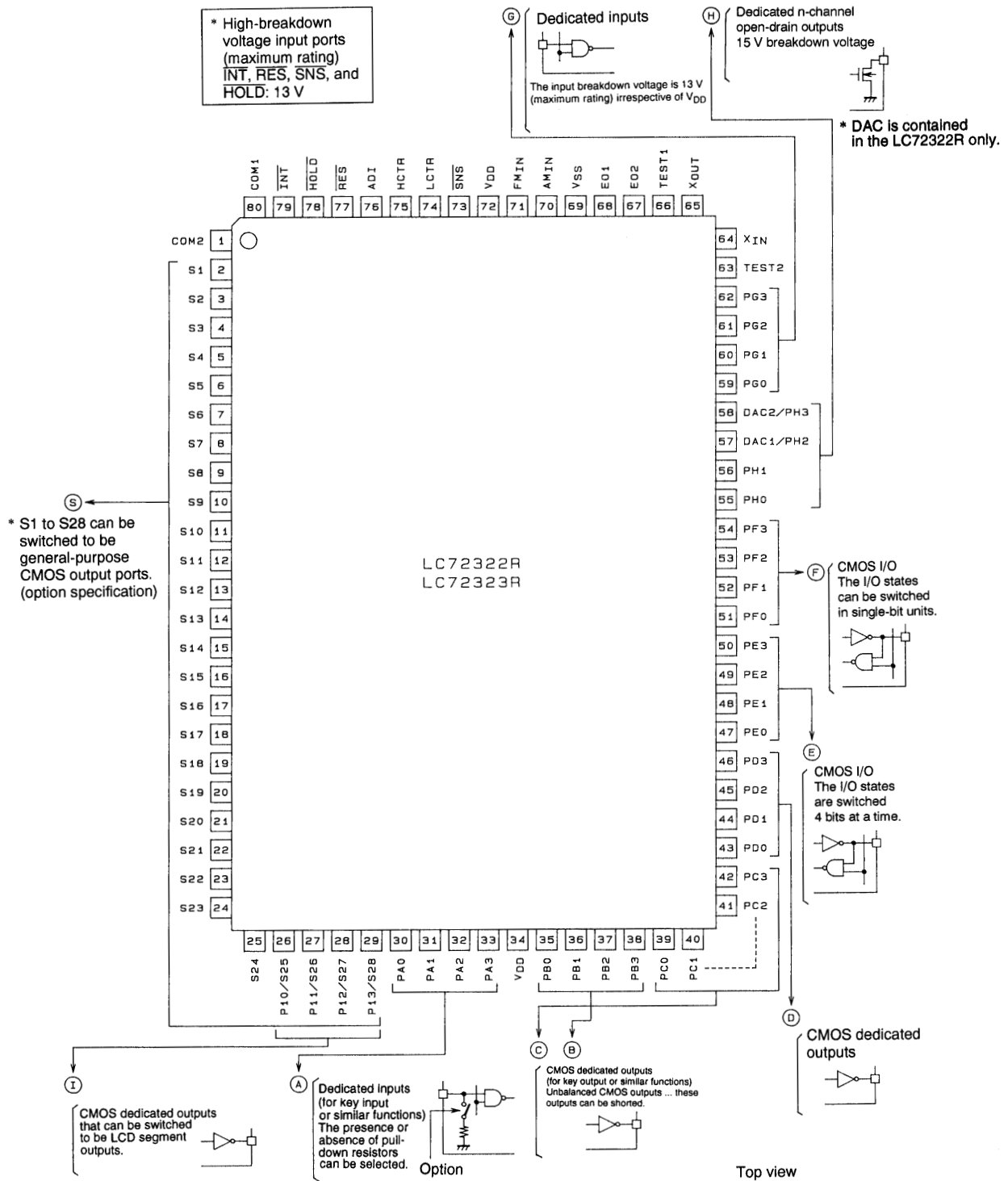
- CCB is a trademark of SANYO ELECTRIC CO., LTD.
- CCB is SANYO's original bus format and all the bus addresses are controlled by SANYO.

**SANYO Electric Co., Ltd. Semiconductor Business Headquarters**

TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110 JAPAN

# LC72322R, 72323R

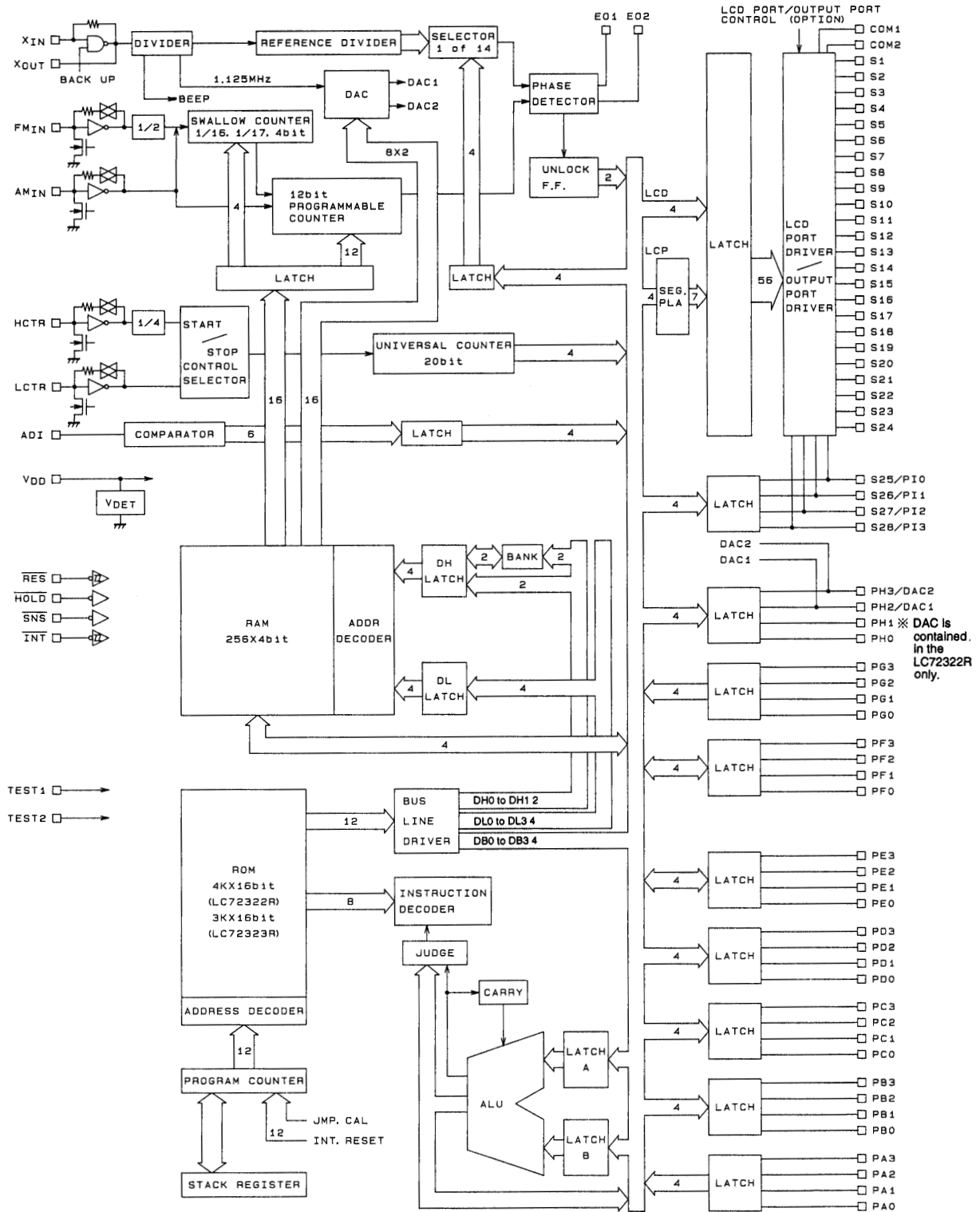
## Pin Assignment



A05276

# LC72322R, 72323R

## Block Diagram



A05275

## Specifications

### Absolute Maximum Ratings at $T_a = 25^\circ\text{C}$ , $V_{SS} = 0\text{ V}$

| Parameter                   | Symbol              | Conditions   | Ratings                | Unit             |
|-----------------------------|---------------------|--|------------------------|------------------|
| Maximum supply voltage      | $V_{DD\text{ max}}$ |  | -0.3 to +6.5           | V                |
| Input voltage               | $V_{IN1}$           | $\overline{\text{HOLD}}$ , $\overline{\text{INT}}$ , $\overline{\text{RES}}$ , ADI, $\overline{\text{SNS}}$ , and the G port | -0.3 to +13            | V                |
|                             | $V_{IN2}$           | Inputs other than $V_{IN1}$  | -0.3 to $V_{DD} + 0.3$ | V                |
| Output voltage              | $V_{OUT1}$          | H port   | -0.3 to +15            | V                |
|                             | $V_{OUT2}$          | Outputs other than $V_{OUT1}$  | -0.3 to $V_{DD} + 0.3$ | V                |
| Output current              | $I_{OUT1}$          | All D and H port pins  | 0 to 5                 | mA               |
|                             | $I_{OUT2}$          | All E and F port pins  | 0 to 3                 | mA               |
|                             | $I_{OUT3}$          | All B and C port pins  | 0 to 1                 | mA               |
|                             | $I_{OUT4}$          | S1 to S28 and all I port pins  | 0 to 1                 | mA               |
| Allowable power dissipation | $Pd\text{ max}$     | $T_a = -40\text{ to }+85^\circ\text{C}$  | 300                    | mW               |
| Operating temperature       | $T_{opr}$           |  | -40 to +85             | $^\circ\text{C}$ |
| Storage temperature         | $T_{stg}$           |  | -45 to +125            | $^\circ\text{C}$ |

### Allowable Operating Ranges at $T_a = -40\text{ to }+85^\circ\text{C}$ , $V_{DD} = 3.5\text{ to }5.5\text{ V}$

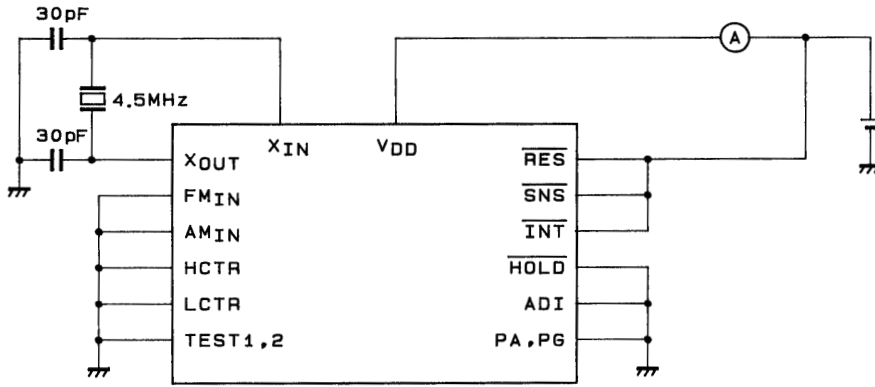
| Parameter                | Symbol       | Conditions   | Ratings      |     |                  | Unit |
|--------------------------|--------------|--|--------------|-----|------------------|------|
|                          |              |  | min          | typ | max              |      |
| Supply voltage           | $V_{DD1}$    | CPU and PLL operating  | 4.5          |     | 5.5              | V    |
|                          | $V_{DD2}$    | CPU operating  | 3.5          |     | 5.5              | V    |
|                          | $V_{DD3}$    | Memory retention voltage   | 1.3          |     | 5.5              | V    |
| Input high level voltage | $V_{IH1}$    | G port   | $0.7 V_{DD}$ |     | 8.0              | V    |
|                          | $V_{IH2}$    | $\overline{\text{RES}}$ , $\overline{\text{INT}}$ , $\overline{\text{HOLD}}$ | $0.8 V_{DD}$ |     | 8.0              | V    |
|                          | $V_{IH3}$    | $\overline{\text{SNS}}$  | 2.5          |     | 8.0              | V    |
|                          | $V_{IH4}$    | A port   | $0.6 V_{DD}$ |     | $V_{DD}$         | V    |
|                          | $V_{IH5}$    | PE0, PE2 and F ports   | $0.7 V_{DD}$ |     | $V_{DD}$         | V    |
|                          | $V_{IH6}$    | LCTR (period measurement), $V_{DD1}$ , PE1 and PE3                           | $0.8 V_{DD}$ |     | $V_{DD}$         | V    |
| Input low level voltage  | $V_{IL1}$    | G port   | 0            |     | $0.3 V_{DD}$     | V    |
|                          | $V_{IL2}$    | $\overline{\text{RES}}$ , $\overline{\text{INT}}$ , PE1, PE3                 | 0            |     | $0.2 V_{DD}$     | V    |
|                          | $V_{IL3}$    | $\overline{\text{SNS}}$  | 0            |     | 1.3              | V    |
|                          | $V_{IL4}$    | A port   | 0            |     | $0.2 V_{DD}$     | V    |
|                          | $V_{IL5}$    | PE0, PE2 and F ports   | 0            |     | $0.3 V_{DD}$     | V    |
|                          | $V_{IL6}$    | LCTR (period measurement), $V_{DD1}$   | 0            |     | $0.2 V_{DD}$     | V    |
|                          | $V_{IL7}$    | $\overline{\text{HOLD}}$   | 0            |     | $0.4 V_{DD}$     | V    |
| Input frequency          | $f_{IN1}$    | XIN  | 4.0          | 4.5 | 5.0              | MHz  |
|                          | $f_{IN2}$    | FMIN, $V_{IN2}$ , $V_{DD1}$  | 10           |     | 130              | MHz  |
|                          | $f_{IN3}$    | FMIN, $V_{IN3}$ , $V_{DD1}$  | 10           |     | 150              | MHz  |
|                          | $f_{IN4}$    | AMIN (L), $V_{IN4}$ , $V_{DD1}$  | 0.5          |     | 10               | MHz  |
|                          | $f_{IN5}$    | AMIN (H), $V_{IN5}$ , $V_{DD1}$  | 2.0          |     | 40               | MHz  |
|                          | $f_{IN6}$    | HCTR, $V_{IN6}$ , $V_{DD1}$  | 0.4          |     | 12               | MHz  |
|                          | $f_{IN7}$    | LCTR (frequency), $V_{IN7}$ , $V_{DD1}$                                      | 100          |     | 500              | kHz  |
|                          | $f_{IN8}$    | LCTR (period), $V_{IH6}$ , $V_{IL6}$ , $V_{DD1}$                             | 1            |     | $20 \times 10^3$ | Hz   |
| Input amplitude          | $V_{IN1}$    | XIN  | 0.50         |     | 1.5              | Vrms |
|                          | $V_{IN2}$    | FMIN   | 0.10         |     | 1.5              | Vrms |
|                          | $V_{IN3}$    | FMIN   | 0.15         |     | 1.5              | Vrms |
|                          | $V_{IN4, 5}$ | AMIN   | 0.10         |     | 1.5              | Vrms |
|                          | $V_{IN6, 7}$ | LCTR, HCTR   | 0.10         |     | 1.5              | Vrms |
| Input voltage range      | $V_{IN8}$    | ADI  | 0            |     | $V_{DD}$         | V    |

## LC72322R, 72323R

### Electrical Characteristics for the Allowable Operating Ranges

| Parameter                             | Symbol  | Conditions   | Ratings              |                |                     | Unit       |
|---------------------------------------|---|--|----------------------|----------------|---------------------|------------|
|                                       |   |  | min                  | typ            | max                 |            |
| Hysteresis                            | $V_H$   | LCTR (period), $\overline{RES}$ , $\overline{INT}$ , PE1, PE3  | 0.1 $V_{DD}$         |                |                     | V          |
| Rejected pulse width                  | $P_{REJ}$   | $\overline{SNS}$   |                      |                | 50                  | $\mu s$    |
| Power-down detection voltage          | $V_{DET}$   |  | 2.7                  | 3.0            | 3.3                 | V          |
| Input high level current              | $I_{IH1}$   | $\overline{INT}$ , $\overline{HOLD}$ , $\overline{RES}$ , $\overline{ADI}$ , $\overline{SNS}$ , and G port: $V_I = 5.5 V$      |                      |                | 3.0                 | $\mu A$    |
|                                       | $I_{IH2}$   | A, E, and F ports: E and F ports with outputs off, A port with no $R_{PD}$ , $V_I = V_{DD}$                                    |                      |                | 3.0                 | $\mu A$    |
|                                       | $I_{IH3}$   | XIN: $V_I = V_{DD} = 5.0 V$  | 2.0                  | 5.0            | 15                  | $\mu A$    |
|                                       | $I_{IH4}$   | FMIN, AMIN, HCTR, LCTR: $V_I = V_{DD} = 5.0 V$   | 4.0                  | 10             | 30                  | $\mu A$    |
|                                       | $I_{IH5}$   | A port: With an $R_{PD}$ , $V_I = V_{DD} = 5.0 V$  |                      | 50             |                     | $\mu A$    |
| Input low level current               | $I_{IL1}$   | $\overline{INT}$ , $\overline{HOLD}$ , $\overline{RES}$ , $\overline{ADI}$ , $\overline{SNS}$ , and the G port: $V_I = V_{SS}$ |                      |                | 3.0                 | $\mu A$    |
|                                       | $I_{IL2}$   | A, E, and F ports: E and F ports with outputs off, A port with no $R_{PD}$ , $V_I = V_{SS}$                                    |                      |                | 3.0                 | $\mu A$    |
|                                       | $I_{IL3}$   | XIN: $V_{IN} = V_{SS}$   | 2.0                  | 5.0            | 15                  | $\mu A$    |
|                                       | $I_{IL4}$   | FMIN, AMIN, HCTR, LCTR: $V_I = V_{SS}$   | 4.0                  | 10             | 30                  | $\mu A$    |
| Input floating voltage                | $V_{IF}$  | A port: With an $R_{PD}$   |                      |                | 0.05 $V_{DD}$       | V          |
| Pull-down resistance                  | $R_{PD}$  | A port: With an $R_{PD}$ , $V_{DD} = 5.0 V$  | 75                   | 100            | 200                 | k $\Omega$ |
| Output high level off leakage current | $I_{OFFH1}$   | EO1, EO2: $V_O = V_{DD}$   |                      | 0.01           | 10                  | nA         |
|                                       | $I_{OFFH2}$   | B, C, D, E, F, and I ports: $V_O = V_{DD}$   |                      |                | 3.0                 | $\mu A$    |
|                                       | $I_{OFFH3}$   | H port: $V_O = V_{DD}$   |                      |                | 5.0                 | $\mu A$    |
| Output low level off leakage current  | $I_{OFFL1}$   | EO1, EO2: $V_O = V_{SS}$   |                      | 0.01           | 10                  | nA         |
|                                       | $I_{OFFL2}$   | B, C, D, E, F, and I ports: $V_O = V_{SS}$   |                      |                | 3.0                 | $\mu A$    |
| Output high level voltage             | $V_{OH1}$   | B and C ports: $I_O = 1 mA$  | $V_{DD} - 2.0$       | $V_{DD} - 1.0$ | $V_{DD} - 0.5$      | V          |
|                                       | $V_{OH2}$   | E and F ports: $I_O = 1 mA$  | $V_{DD} - 1.0$       |                |                     | V          |
|                                       | $V_{OH3}$   | EO1, EO2: $I_O = 500 \mu A$  | $V_{DD} - 1.0$       |                |                     | V          |
|                                       | $V_{OH4}$   | XOUT: $I_O = 200 \mu A$  | $V_{DD} - 1.0$       |                |                     | V          |
|                                       | $V_{OH5}$   | S1 to S28 and the I port: $I_O = -0.1 mA$  | $V_{DD} - 1.0$       |                |                     | V          |
|                                       | $V_{OH6}$   | D port: $I_O = 5 mA$   | $V_{DD} - 1.0$       |                |                     | V          |
|                                       | $V_{OH7}$   | COM1, COM2: $I_O = 25 \mu A$   | $V_{DD} - 0.75$      | $V_{DD} - 0.5$ | $V_{DD} - 0.3$      | V          |
| Output low level voltage              | $V_{OL1}$   | B and C ports: $I_O = 50 \mu A$  | 0.5                  | 1.0            | 2.0                 | V          |
|                                       | $V_{OL2}$   | E and F ports: $I_O = 1 mA$  |                      |                | 1.0                 | V          |
|                                       | $V_{OL3}$   | EO1, EO2: $I_O = 500 \mu A$  |                      |                | 1.0                 | V          |
|                                       | $V_{OL4}$   | XOUT: $I_O = 200 \mu A$  |                      |                | 1.0                 | V          |
|                                       | $V_{OL5}$   | S1 to S28 and the I port: $I_O = 0.1 mA$   |                      |                | 1.0                 | V          |
|                                       | $V_{OL6}$   | D port: $I_O = 5 mA$   |                      |                | 1.0                 | V          |
|                                       | $V_{OL7}$   | COM1, COM2: $I_O = 25 \mu A$   | 0.3                  | 0.5            | 0.75                | V          |
|                                       | $V_{OL8}$   | H port: $I_O = 5 mA$ , $V_{DD1}$   | (150 $\Omega$ ) 0.75 |                | (400 $\Omega$ ) 2.0 | V          |
| Output middle level voltage           | $V_M1$  | COM1, COM2: $V_{DD} = 5.0 V$ , $I_O = 25 \mu A$  | 2.0                  | 2.5            | 3.0                 | V          |
| A/D conversion error                  |   | ADI: $V_{DD1}$   | -1/2                 |                | +1/2                | LSB        |
| Current drain                         | $I_{DD1}$   | $V_{DD1}$ , $f_{IN2} = 130 MHz$  |                      | 15             | 20                  | mA         |
|                                       | $I_{DD2}$   | $V_{DD2}$ , PLL stopped, CT = 2.67 $\mu s$ (HOLD mode, Figure 1)   |                      | 1.5            |                     | mA         |
|                                       | $I_{DD3}$   | $V_{DD2}$ , PLL stopped, CT = 13.33 $\mu s$ (HOLD mode, Figure 1)  |                      | 1.0            |                     | mA         |
|                                       | $I_{DD4}$   | $V_{DD2}$ , PLL stopped, CT = 40.00 $\mu s$ (HOLD mode, Figure 1)  |                      | 0.7            |                     | mA         |
|                                       | $I_{DD5}$   | $V_{DD} = 5.5 V$ , oscillator stopped, Ta = 25°C (BACK UP mode, Figure 2)  |                      |                | 5                   | $\mu A$    |
|                                       | $V_{DD} = 2.5 V$ , oscillator stopped, Ta = 25°C (BACK UP mode, Figure 2) |  |                      | 1              | $\mu A$             |            |

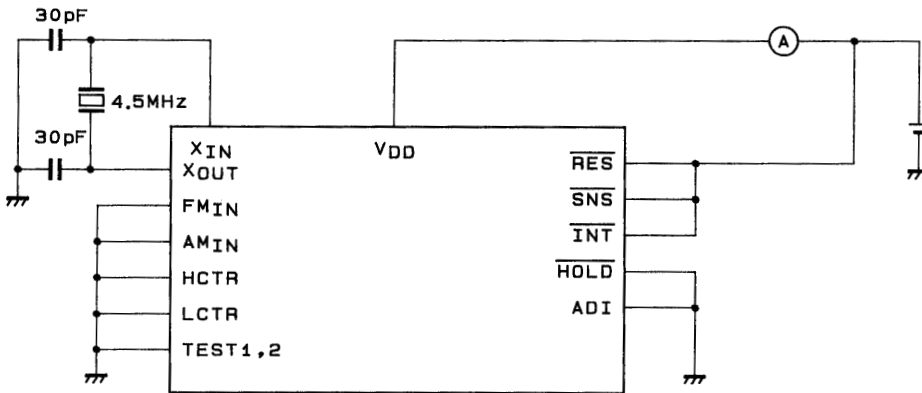
Test Circuits



A02105

Note: PB to PF, PH, and PI are all open. However, PE and PF are specified as output.

Figure 1  $I_{DD2}$  to  $I_{DD4}$  in HOLD Mode



Note: PA to PI, S1 to S4, COM1, and COM2 are all open.

Figure 2  $I_{DD5}$  in BACK UP Mode

Pin Functions

| Pin  | Pin No.                                      | Functions   | I/O    | I/O circuit type |
|--|--|---|--------|------------------|
| PA0<br>PA1<br>PA2<br>PA3                             | 30<br>31<br>32<br>33                         | Low-threshold type dedicated input ports<br>These pins can be used, for example, for key data acquisition.<br>Built-in pull-down resistors can be specified as an option. This option is in 4-pin units, and cannot be specified for individual pins.<br>Input through these pins is disabled in BACKUP mode.   | Input  | <p>A02107</p>    |
| PB0<br>PB1<br>PB2<br>PB3<br>PC0<br>PC1<br>PC2<br>PC3 | 35<br>36<br>37<br>38<br>39<br>40<br>41<br>42 | Dedicated output ports<br>Since the output transistor impedances are unbalanced CMOS, these pins can be effectively used for functions such as key scan timing. These pins go to the output high-impedance state in BACKUP mode.<br>These pins go to the low level during a reset, i.e., when the RES pin is low.   | Output | <p>A02108</p>    |
| PD0<br>PD1<br>PD2<br>PD3                             | 43<br>44<br>45<br>46                         | Dedicated output ports<br>These are normal CMOS outputs. These pins go to the output high-impedance state in BACKUP mode.<br>These pins go to the low level during a reset, i.e., when the RES pin is low.  |        | <p>A02109</p>    |
| PE0<br>PE1<br>PE2<br>PE3                             | 47<br>48<br>49<br>50                         | I/O ports<br>These pins are switched between input and output as follows: Once an input instruction (IN, TPT, or TPF) is executed, these pins latch in the input mode. Once an output instruction (OUT, SPB, or RPB) is executed, they latch in the output mode.<br>These pins go to the input mode during a reset, i.e., when the RES pin is low.<br>In BACKUP mode these pins go to the input mode with input disabled. | I/O    | <p>A02110</p>    |
| PF0<br>PF1<br>PF2<br>PF3                             | 51<br>52<br>53<br>54                         | I/O ports<br>These pins are switched between input and output by the FPC instruction.<br>The I/O states of this port can be specified for individual pins.<br>These pins go to the input mode during a reset, i.e., when the RES pin is low.<br>In BACKUP mode these pins go to the input mode with input disabled.   |        | <p>A02111</p>    |
| PG0<br>PG1<br>PG2<br>PG3                             | 59<br>60<br>61<br>62                         | Dedicated input ports<br>Input through these pins is disabled in BACKUP mode.   | Input  | <p>A02111</p>    |

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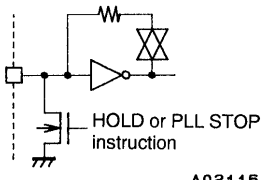
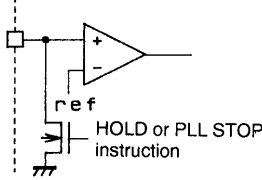
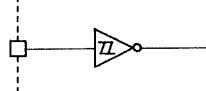
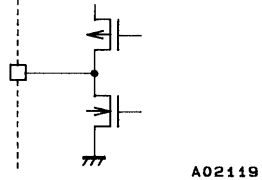
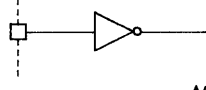
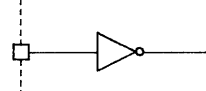
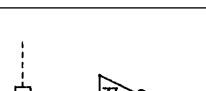
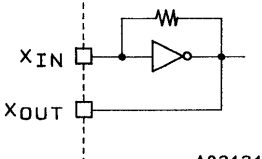
| Pin                                      | Pin No.              | Functions   | I/O    | I/O circuit type                         |
|--|----------------------|---|--------|--|
| PH0<br>PH1<br>PH2/DAC*1<br>PH3/DAC*2     | 55<br>56<br>57<br>58 | <p>Dedicated output ports</p> <p>Since these pins are high-breakdown voltage n-channel transistor open-drain outputs, they can be effectively used for functions such as band power supply switching.</p> <p>And, PH2 and PH3 can also be used for DAC1 and DAC2 output ports respectively. (*: DAC is contained in LC72322R only.)</p> <p>These ports go to the high impedance state during a reset, i.e., when the <math>\overline{\text{RES}}</math> pin is low, and in BACKUP mode.</p>   | Output | <p style="text-align: right;">A02112</p> |
| PI0/S25<br>PI1/S26<br>PI2/S27<br>PI3/S28 | 26<br>27<br>28<br>29 | <p>Dedicated output ports</p> <p>While these pins have a CMOS output circuit structure, they can be switched to function as LCD drivers. Their function is switched by the SS and RS instructions. These pins cannot be switched individually.</p> <p>The LCD driver function is selected and a segment-off signal is output when power is first applied or when <math>\overline{\text{RES}}</math> is low.</p> <p>These pins are held at the low level in BACKUP mode.</p> <p>Note that when the general-purpose port use option is specified, these pins output the contents of IPORT when LPC is 1, and the contents of the general-purpose output port LATCH when LPC is 0.</p> | Output | <p style="text-align: right;">A02113</p> |
| S1 to S24                                | 2 to 25              | <p>LCD driver segment outputs</p> <p>A frame frequency of 100 Hz and a 1/2 duty, 1/2 bias drive type are used.</p> <p>A segment-off signal is output when power is first applied or when <math>\overline{\text{RES}}</math> is low.</p> <p>These pins are held at the low level in BACKUP mode.</p> <p>The use of these pins as general-purpose output ports can be specified as an option.</p>   | Output | <p style="text-align: right;">A02114</p> |
| COM1<br>COM2                             | 80<br>1              | <p>LCD driver common outputs</p> <p>A 1/2 duty, 1/2 bias drive type is used.</p> <p>The output when power is first applied or when <math>\overline{\text{RES}}</math> is low is identical to the normal operating mode output.</p> <p>These pins are held at the low level in BACKUP mode.</p>  | Output | <p style="text-align: right;">A02115</p> |
| FMIN                                     | 71                   | <p>FM VCO (local oscillator) input</p> <p>The input must be capacitor coupled.</p> <p>The input frequency range is from 10 to 130 MHz. (Max. 150 MHz)</p>   | Input  | <p style="text-align: right;">A02116</p> |
| AMIN                                     | 70                   | <p>AM VCO (local oscillator) input</p> <p>The input must be capacitor coupled</p> <p>The band supported by this pin can be selected using the PLL instruction.</p> <p>High (2 to 40 MHz) → SW</p> <p>Low (0.5 to 10 MHz) → LW and MW</p>  |        |  |

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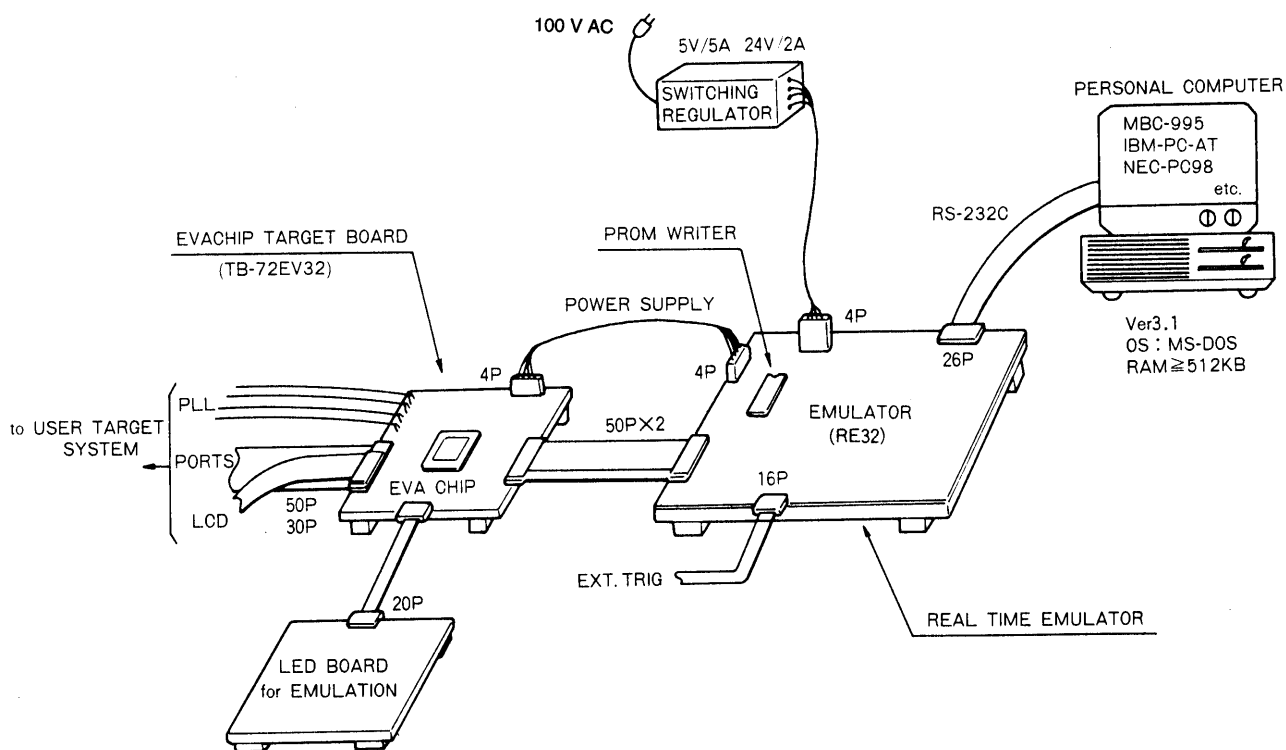
| Pin                      | Pin No.      | Functions  | I/O             | I/O circuit type  |
|--------------------------|--------------|--|-----------------|---|
| HCTR                     | 75           | Universal counter input<br>The input must be capacitor coupled.<br>The input frequency range is from 0.4 to 12 MHz.<br>This input can be effectively used for FM IF or AM IF counting.   | Input           |    |
| LCTR                     | 74           | Universal counter input<br>The input must be capacitor coupled for input frequencies in the range 100 to 150 kHz.<br>Capacitor coupling is not required for input frequencies from 1 Hz to 20 kHz.<br>This input can be effectively used for AM IF counting.   |                 |   |
| ADI                      | 76           | A/D converter input<br>A 1.28 ms period is required for a 6-bit sequential comparison conversion. The full scale input is $((63/96) \cdot V_{DD})$ for a data value of 3FH.  | Input           |    |
| INT                      | 79           | External interrupt request input<br>An interrupt is generated when the INTEN flag is set (by an SS instruction) and a falling edge is input.   | Input           |   |
| EO1<br>EO2               | 68<br>67     | Reference frequency and programmable divider phase comparison error outputs<br>Charge pump circuits are built in.<br>EO1 and EO2 are the same.   | Output          |  |
| $\overline{\text{SNS}}$  | 73           | Input pin used to determine if a power outage has occurred in BACKUP mode<br>This pin can also be used as a normal input port.   | Input           |  |
| $\overline{\text{HOLD}}$ | 78           | Input pin used to force the ICs to HOLD mode<br>The IC goes to HOLD mode when the HOLDEN flag is set (by an SS instruction) and the $\overline{\text{HOLD}}$ input goes low.<br>A high-breakdown voltage circuit is used so that this input can be used in conjunction with the normal power switch. | Input           |  |
| $\overline{\text{RES}}$  | 77           | System reset input<br>This signal should be held low for 75 ms after power is first applied to effect a power-up reset.<br>The reset starts when a low level has been input for at least six reference clock cycles.   | Input           |  |
| XIN<br>XOUT              | 64<br>65     | Crystal oscillator connections<br>(4.5 MHz)<br>A feedback resistor is built in.  | Input<br>Output |  |
| TEST1<br>TEST2           | 66<br>63     | LSI test pins. These pins must be connected to $V_{SS}$ .  | —               |   |
| $V_{DD}$<br>$V_{SS}$     | 34, 72<br>69 | Power supply   | —               |   |

### Mask Options

| No. | Description                                   | Selections                   |
|-----|---|------------------------------|
| 1   | WDT (watchdog timer) inclusion selection      | WDT included                 |
|     |   | No WDT                       |
| 2   | Port A pull-down resistor inclusion selection | Pull-down resistors included |
|     |   | No pull-down resistors       |
| 3   | Cycle time selection                          | 2.67 $\mu$ s                 |
|     |   | 13.33 $\mu$ s                |
|     |   | 40.00 $\mu$ s                |
| 4   | LCD port/general-purpose port selection       | LCD ports                    |
|     |   | General-purpose output ports |

### Development Environment

- The LC72P321R is used for OTP.
- The LC72EV321 is used as the evaluation chip.
- A total debugging system is available in which the TB-72EV32 evaluation chip board and the RE32 multifunction emulator are controlled by a personal computer.



**LC72322R, 72323R Instruction Table**

Abbreviations:

- ADDR: Program memory address [12 bits]
- b: Borrow
- B: Bank number [2 bits]
- C: Carry
- DH: Data memory address high (row address) [2 bits]
- DL: Data memory address low (column address) [4 bits]
- I: Immediate data [4 bits]
- M: Data memory address
- N: Bit position [4 bits]
- Pn: Port number [4 bits]
- r: General register (one of the locations 00 to 0FH in bank 0)
- Rn: Register number [4 bits]
- ( ): Contents of register or memory
- ( )N: Contents of bit N of register or memory

| Instruction Group        | Mnemonic | Operand |     | Function   | Operation                                       | Machine code |    |    |    |    |    |    |    |    |   |   |   |
|--------------------------|----------|---------|-----|--|---|--------------|----|----|----|----|----|----|----|----|---|---|---|
|                          |          | 1st     | 2nd |  |   | D15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6 | 5 | 4 |
| Addition instructions    | AD       | r       | M   | Add M to r   | $r \leftarrow (r) + (M)$                        | 0            | 1  | 0  | 0  | 0  | 0  | DH | DL | Rn |   |   |   |
|                          | ADS      | r       | M   | Add M to r, then skip if carry                     | $r \leftarrow (r) + (M)$<br>skip if carry       | 0            | 1  | 0  | 0  | 0  | 1  | DH | DL | Rn |   |   |   |
|                          | AC       | r       | M   | Add M to r with carry                              | $r \leftarrow (r) + (M) + C$                    | 0            | 1  | 0  | 0  | 1  | 0  | DH | DL | Rn |   |   |   |
|                          | ACS      | r       | M   | Add M to r with carry, then skip if carry          | $r \leftarrow (r) + (M) + C$<br>skip if carry   | 0            | 1  | 0  | 0  | 1  | 1  | DH | DL | Rn |   |   |   |
|                          | AI       | M       | I   | Add I to M   | $M \leftarrow (M) + I$                          | 0            | 1  | 0  | 1  | 0  | 0  | DH | DL | I  |   |   |   |
|                          | AIS      | M       | I   | Add I to M, then skip if carry                     | $M \leftarrow (M) + I$<br>skip if carry         | 0            | 1  | 0  | 1  | 0  | 1  | DH | DL | I  |   |   |   |
|                          | AIC      | M       | I   | Add I to M with carry                              | $M \leftarrow (M) + I + C$                      | 0            | 1  | 0  | 1  | 1  | 0  | DH | DL | I  |   |   |   |
|                          | AICS     | M       | I   | Add I to M with carry, then skip if carry          | $M \leftarrow (M) + I + C$<br>skip if carry     | 0            | 1  | 0  | 1  | 1  | 1  | DH | DL | I  |   |   |   |
| Subtraction instructions | SU       | r       | M   | Subtract M from r                                  | $r \leftarrow (r) - (M)$                        | 0            | 1  | 1  | 0  | 0  | 0  | DH | DL | Rn |   |   |   |
|                          | SUS      | r       | M   | Subtract M from r, then skip if borrow             | $r \leftarrow (r) - (M)$<br>skip if borrow      | 0            | 1  | 1  | 0  | 0  | 1  | DH | DL | Rn |   |   |   |
|                          | SB       | r       | M   | Subtract M from r with borrow                      | $r \leftarrow (r) - (M) - b$                    | 0            | 1  | 1  | 0  | 1  | 0  | DH | DL | Rn |   |   |   |
|                          | SBS      | r       | M   | Subtract M from r with borrow, then skip if borrow | $r \leftarrow (r) - (M) - b$<br>skip if borrow  | 0            | 1  | 1  | 0  | 1  | 1  | DH | DL | Rn |   |   |   |
|                          | SI       | M       | I   | Subtract I from M                                  | $M \leftarrow (M) - I$                          | 0            | 1  | 1  | 1  | 0  | 0  | DH | DL | I  |   |   |   |
|                          | SIS      | M       | I   | Subtract I from M, then skip if borrow             | $M \leftarrow (M) - I$<br>skip if borrow        | 0            | 1  | 1  | 1  | 0  | 1  | DH | DL | I  |   |   |   |
|                          | SIB      | M       | I   | Subtract I from M with borrow                      | $M \leftarrow (M) - I - b$                      | 0            | 1  | 1  | 1  | 1  | 0  | DH | DL | I  |   |   |   |
|                          | SIBS     | M       | I   | Subtract I from M with borrow, then skip if borrow | $M \leftarrow (M) - I - b$<br>skip if borrow    | 0            | 1  | 1  | 1  | 1  | 1  | DH | DL | I  |   |   |   |
| Comparison instructions  | SEQ      | r       | M   | Skip if r equals M                                 | $r - M$<br>skip if zero                         | 0            | 0  | 0  | 0  | 0  | 1  | DH | DL | Rn |   |   |   |
|                          | SGE      | r       | M   | Skip if r is greater than or equal to M            | $r - M$<br>skip if not borrow<br>$(r) \geq (M)$ | 0            | 0  | 0  | 0  | 1  | 1  | DH | DL | Rn |   |   |   |
|                          | SEQL     | M       | I   | Skip if M equal to I                               | $M - I$<br>skip if zero                         | 0            | 0  | 1  | 1  | 0  | 1  | DH | DL | I  |   |   |   |
|                          | SGEL     | M       | I   | Skip if M is greater than or equal to I            | $M - I$<br>skip if not borrow<br>$(M) \geq I$   | 0            | 0  | 1  | 1  | 1  | 1  | DH | DL | I  |   |   |   |

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| Instruction Group              | Mnemonic | Operand |     | Function   | Operation  | Machine code |    |    |    |                |    |    |   |     |   |     |   |   |   |   |    |
|--------------------------------|----------|---------|-----|--|--|--------------|----|----|----|----------------|----|----|---|-----|---|-----|---|---|---|---|----|
|                                |          | 1st     | 2nd |  |  | D15          | 14 | 13 | 12 | 11             | 10 | 9  | 8 | 7   | 6 | 5   | 4 | 3 | 2 | 1 | D0 |
| Logical operation instructions | AND      | M       | I   | AND I with M   | $M \leftarrow (M) \wedge I$  | 0            | 0  | 1  | 1  | 0              | 0  | DH |   | DL  |   | I   |   |   |   |   |    |
|                                | OR       | M       | I   | OR I with M  | $M \leftarrow (M) \vee I$  | 0            | 0  | 1  | 1  | 1              | 0  | DH |   | DL  |   | I   |   |   |   |   |    |
|                                | EXL      | r       | M   | Exclusive OR M with r                                  | $r \leftarrow (r) \oplus (M)$  | 0            | 0  | 1  | 0  | 0              | 0  | DH |   | DL  |   | Rn  |   |   |   |   |    |
| Transfer instructions          | LD       | r       | M   | Load M to r  | $r \leftarrow (M)$   | 1            | 0  | 0  | 0  | 0              | 0  | DH |   | DL  |   | Rn  |   |   |   |   |    |
|                                | ST       | M       | r   | Store r to M   | $M \leftarrow (r)$   | 1            | 0  | 0  | 0  | 0              | 1  | DH |   | DL  |   | Rn  |   |   |   |   |    |
|                                | MVRD     | r       | M   | Move M to destination M referring to r in the same row | $[DH, Rn] \leftarrow (M)$  | 1            | 0  | 0  | 0  | 1              | 0  | DH |   | DL  |   | Rn  |   |   |   |   |    |
|                                | MVRS     | M       | r   | Move source M referring to r to M in the same row      | $M \leftarrow [DH, Rn]$  | 1            | 0  | 0  | 0  | 1              | 1  | DH |   | DL  |   | Rn  |   |   |   |   |    |
|                                | MVSR     | M1      | M2  | Move M to M in the same row                            | $[DH, DL1] \leftarrow [DH, DL2]$   | 1            | 0  | 0  | 1  | 0              | 0  | DH |   | DL1 |   | DL2 |   |   |   |   |    |
|                                | MVI      | M       | I   | Move I to M  | $M \leftarrow I$   | 1            | 0  | 0  | 1  | 0              | 1  | DH |   | DL  |   | I   |   |   |   |   |    |
|                                | PLL      | M       | r   | Load M to PLL registers                                | $PLL\ r \leftarrow PLL\ DATA$  | 1            | 0  | 0  | 1  | 1              | 0  | DH |   | DL  |   | Rn  |   |   |   |   |    |
| Bit test instructions          | TMT      | M       | N   | Test M bits, then skip if all bits specified are true  | if $M(N) = \text{all } 1$ , then skip  | 1            | 0  | 1  | 0  | 0              | 1  | DH |   | DL  |   | N   |   |   |   |   |    |
|                                | TMF      | M       | N   | Test M bits, then skip if all bits specified are false | if $M(N) = \text{all } 0$ , then skip  | 1            | 0  | 1  | 0  | 1              | 1  | DH |   | DL  |   | N   |   |   |   |   |    |
| Jump and subroutine call       | JMP      | ADDR    |     | Jump to the address                                    | $PC \leftarrow ADDR$   | 1            | 0  | 1  | 1  | ADDR (12 bits) |    |    |   |     |   |     |   |   |   |   |    |
|                                | CAL      | ADDR    |     | Call subroutine  | $Stack \leftarrow (PC) + 1$  | 1            | 1  | 0  | 0  | ADDR (12 bits) |    |    |   |     |   |     |   |   |   |   |    |
|                                | RT       |         |     | Return from subroutine                                 | $PC \leftarrow Stack$  | 1            | 1  | 0  | 1  | 0              | 1  | 0  | 0 | 0   | 0 | 0   | 0 | 0 | 0 | 0 | 0  |
|                                | RTI      |         |     | Return from interrupt                                  | $BANK \leftarrow Stack$<br>$PC \leftarrow Stack$<br>$CARRY \leftarrow Stack$ | 1            | 1  | 0  | 1  | 0              | 1  | 0  | 1 | 0   | 0 | 0   | 0 | 0 | 0 | 0 | 0  |
| F/F test instructions          | TTM      | N       |     | Test timer F/F then skip if it has not been set        | if timer $F/F = 0$ , then skip   | 1            | 1  | 0  | 1  | 0              | 1  | 1  | 0 | 0   | 0 | 0   | 0 | N |   |   |    |
|                                | TUL      | N       |     | Test unlock F/F then skip if it has not been set       | if $UL\ F/F = 0$ , then skip   | 1            | 1  | 0  | 1  | 0              | 1  | 1  | 1 | 0   | 0 | 0   | 0 | N |   |   |    |
| Status register instructions   | SS       | N       |     | Set status register                                    | (Status register 1)<br>$N \leftarrow 1$                                      | 1            | 1  | 0  | 1  | 1              | 1  | 0  | 0 | 0   | 0 | 0   | 0 | N |   |   |    |
|                                | RS       | N       |     | Reset status register                                  | (Status register 1)<br>$N \leftarrow 0$                                      | 1            | 1  | 0  | 1  | 1              | 1  | 0  | 1 | 0   | 0 | 0   | 0 | N |   |   |    |
|                                | TST      | N       |     | Test status register true                              | if (Status register 2) $N = \text{all } 1$ , then skip                       | 1            | 1  | 0  | 1  | 1              | 1  | 1  | 0 | 0   | 0 | 0   | 0 | N |   |   |    |
|                                | TSF      | N       |     | Test status register false                             | if (Status register 2) $N = \text{all } 0$ , then skip                       | 1            | 1  | 0  | 1  | 1              | 1  | 1  | 1 | 0   | 0 | 0   | 0 | N |   |   |    |
| Bank switching instructions    | BANK     | B       |     | Select bank  | $BANK \leftarrow B$  | 1            | 1  | 0  | 1  | 0              | 0  | B  |   | 0   | 0 | 0   | 0 | 0 | 0 | 0 |    |

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| Instruction Group              | Mnemonic | Operand |     | Function  | Operation                           | Machine code |    |    |    |    |    |    |    |       |   |   |   |   |   |   |    |
|--------------------------------|----------|---------|-----|---|-------------------------------------|--------------|----|----|----|----|----|----|----|-------|---|---|---|---|---|---|----|
|                                |          | 1st     | 2nd |   |                                     | D15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7     | 6 | 5 | 4 | 3 | 2 | 1 | D0 |
| I/O instructions               | LCD      | M       | I   | Output segment pattern to LCD digit direct                | LCD (DIGIT) ← M                     | 1            | 1  | 1  | 0  | 0  | 0  | DH | DL | DIGIT |   |   |   |   |   |   |    |
|                                | LCP      | M       | I   | Output segment pattern to LCD digit through PLA           | LCD (DIGIT) ← PLA ← M               | 1            | 1  | 1  | 0  | 0  | 1  | DH | DL | DIGIT |   |   |   |   |   |   |    |
|                                | IN       | M       | P   | Input port data to M                                      | M ← (Port (P))                      | 1            | 1  | 1  | 0  | 1  | 0  | DH | DL | P     |   |   |   |   |   |   |    |
|                                | OUT      | M       | P   | Output contents of M to port                              | (Port (P)) ← M                      | 1            | 1  | 1  | 0  | 1  | 1  | DH | DL | P     |   |   |   |   |   |   |    |
|                                | SPB      | P       | N   | Set port bits   | (Port (P)) N ← 1                    | 1            | 1  | 1  | 1  | 0  | 0  | 0  | 0  | P     | N |   |   |   |   |   |    |
|                                | RPB      | P       | N   | Reset port bits   | (Port (P)) N ← 0                    | 1            | 1  | 1  | 1  | 0  | 1  | 0  | 1  | P     | N |   |   |   |   |   |    |
|                                | TPT      | P       | N   | Test port bits, then skip if all bits specified are true  | if (Port (P)) N = all 1, then skip  | 1            | 1  | 1  | 1  | 1  | 0  | 1  | 0  | P     | N |   |   |   |   |   |    |
|                                | TPF      | P       | N   | Test port bits, then skip if all bits specified are false | if (Port (P)) N = all 0, then skip  | 1            | 1  | 1  | 1  | 1  | 1  | 1  | 1  | P     | N |   |   |   |   |   |    |
| Universal counter instructions | UCS      | I       |     | Set I to UCCW1  | UCCW1 ← I                           | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0     | 0 | 0 | 0 | I |   |   |    |
|                                | UCC      | I       |     | Set I to UCCW2  | UCCW2 ← I                           | 0            | 0  | 0  | 0  | 0  | 0  | 1  | 1  | 0     | 0 | 0 | 0 | I |   |   |    |
| Other instructions             | FPC      | N       |     | F port I/O control  | FPC latch ← N                       | 0            | 0  | 0  | 1  | 0  | 0  | 0  | 0  | 0     | 0 | 0 | 0 | N |   |   |    |
|                                | CKSTP    |         |     | Clock stop  | Stop clock if $\overline{HOLD} = 0$ | 0            | 0  | 0  | 1  | 0  | 0  | 0  | 1  | 0     | 0 | 0 | 0 | 0 | 0 | 0 |    |
|                                | DAC*     | I       |     | Load M to D/A registers                                   | DA reg ← DAC DATA                   | 0            | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0     | 0 | 0 | 0 | I |   |   |    |
|                                | NOP      |         |     | No operation  |                                     | 0            | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0     | 0 | 0 | 0 | 0 | 0 | 0 |    |

Note: \* DAC is contained in LC72322R only.

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