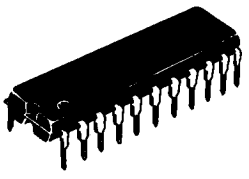
HD42853

PLL FREQUENCY SYNTHESIZER

The HD42853 incorporates the following functions:

- Reference oscillation circuit (10.24MHz crystal oscillator externally mounted)
- Divider (N=2048 in AM; N=1024 in SSB)
- Programmable divider (BCD code)
- Phase detector
- Amplifier for active filter (open drain type)
- Handset cord converter
- SSB 1/2 divider
- Amplifier for unlock output filter



(DP-22)

■ FEATURES

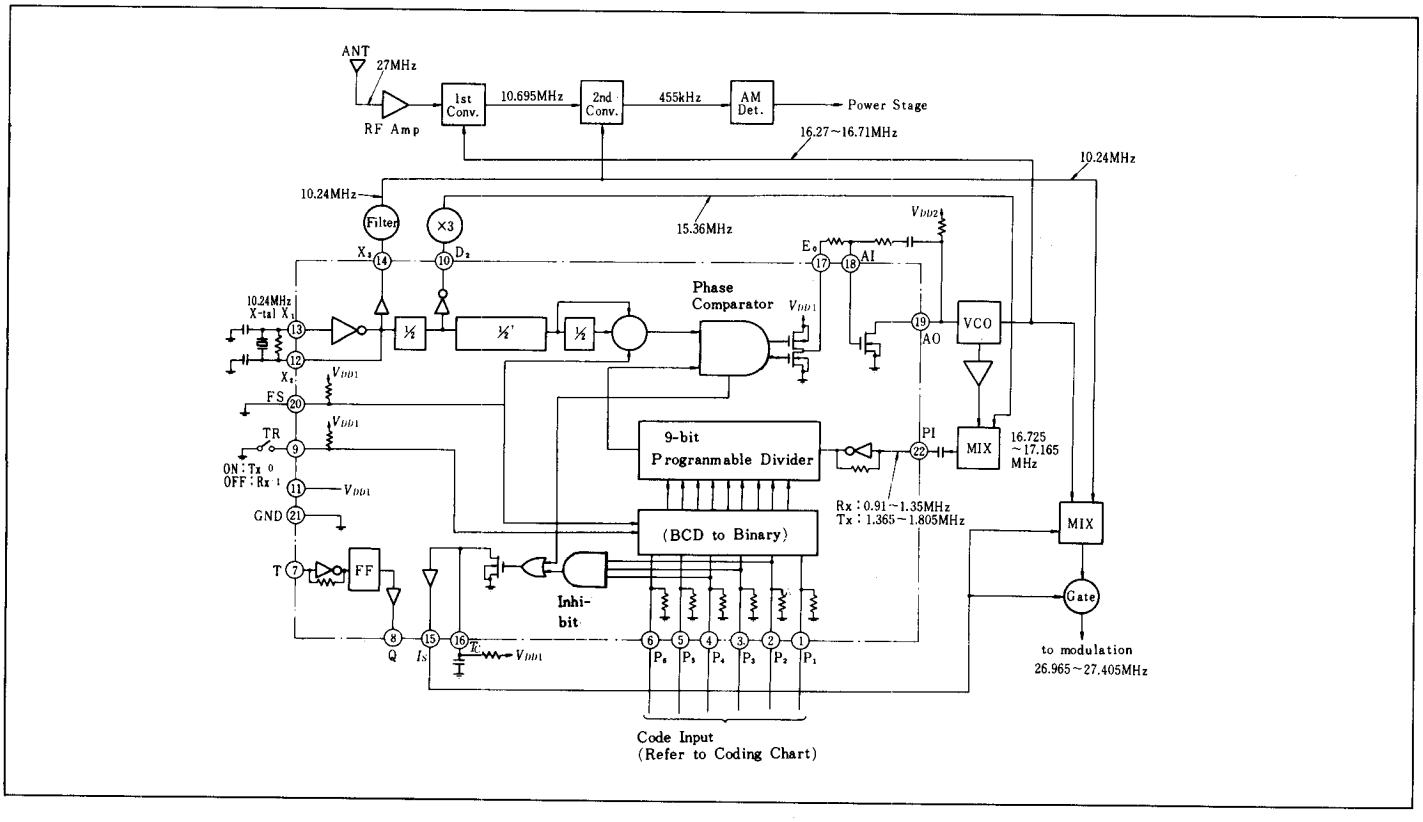
- A 40-channel AM transceiver system may be constructed by use of one 10.2MHz crystal oscillator.

  Frequencies that can be generated are:

Transmitting carrier	26.965 to 27.405MHz
Receiving 1st local oscillation	16.27 to 16.71MHz
Receiving 2nd local oscillation	10.24MHz

- The unlock output (with filter) and 40-channel external prohibit signal output terminal (pin ⑮) prevents out-of-band radiation. When a code other than that of 40-channels comes, the double safety measures are taken because one channel of programmable divider only is used.
- Since an amplifier for high input impedance active filter is incorporated, the filter hold time is long and spurious radiation can be improved to a significant extent. Also, as this IC is an MOS open drain type with withstand voltage of 20V, the dynamic range for the voltage control oscillator can be increased.
- As internal bias is applied to the programmable divider input terminal (pin ㉒) and the SSB 1/2 divider input terminal (pin ⑦), and operation is made at an input of 100mV rms, an external amplifier is not required.
- A pull-down resistor is built in the channel selector pins (pin ① – ⑥). Also, a pull-up resistor is built in the send/receive selector input pin (pin ⑨) and AM/SSB selector pin (pin ⑳).
- Two 10.24MHz crystal oscillators and one 11.15MHz crystal oscillator are used to provide a SSB system.
- A scanner system can be constructed when this circuit is used in combination with the channel selector scanner ICs, HD42854 and HD42855.

■ BLOCK DIAGRAM (AM Transceiver)



■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	HD42853	Unit
Supply Voltage	V_{DD1}*	−0.3 to +6.0	V
	V_{DD2}**	−0.3 to +20	V
Input Voltage	V_{in}	−0.3 to +6.3	V
Operating Temperature	T_{opr}	−35 to +75	°C
Storage Temperature	T_{stg}	−55 to +125	°C

*; pin 11 and 16
**; Pin 19

■ ELECTRICAL CHARACTERISTICS (Ta = −35 to +75°C)

Item	Symbol	Test Condition	min	typ	max	Unit
Supply Voltage	V_{DD}		4.5	5.0	5.5	V
Input Voltage	V_{IH}	①to⑥, ⑨, ⑳	0.8V_{DD}	—	—	V
	V_{IL}		—	—	0.2V_{DD}	V
Output Voltage	V_{OH}	⑭, ⑮, I_{OH} = −2.5mA, V_{DD} = 4.5V	3.8	—	—	V
		⑧, ⑩, ⑰, I_{OH} = −0.5mA, V_{DD} = 4.5V	3.8	—	—	
	V_{OL}	⑭, ⑮, I_{OL} = 2.5mA, V_{DD} = 4.5V	—	—	0.7	V
		⑧, ⑯, ⑰, ⑲, I_{OL} = 0.7mA, V_{DD} = 4.5V	—	—	0.7	
		⑩, I_{OL} = 1.6mA, V_{DD} = 4.5V	—	—	0.4	
Input Current	I_{IH}	①to⑥, V_{DD} = 5.5V, V_{in} = 5.5V	—	—	0.5	mA
	I_{IL}	⑨, ⑳, V_{DD} = 5.5V	−0.5	—	—	mA
Max. Operating Frequency (Programmable Divider)	f_P max	Input 0.28Vp-p Sine Wave, V_{DD} = 4.5V	3.3	—	—	MHz
Max. Operating Frequency (OSC Divider)	f_D max	X-tal between pin 12 and 13, V_{DD} = 4.5V	11	—	—	MHz
Max. Operating Frequency (1/2 Divider)	f_T max	Input 0.28Vp-p Sine Wave, V_{DD} = 4.5V	6	—	—	MHz
Pin 19 Leak Current	I_L	V_{19} = 12V, ⑱ = 0V, V_{DD} = 5.5V	—	10	—	nA
Pin 16 Leak Current		V_{16} = 1V, ②, ③, ④ = 1, V_{DD} = 5.5V	—	10	—	
Leak Current between pin 17 and 18		Connect to pin18 and opened pin17, V_{DD} = 5.5V	—	1.0	—	
Input Capacitance	C_{in}	①to⑥, ⑱, ⑬, ⑨, ⑦, ⑳, ㉒	—	8	—	pF

■ DESCRIPTION OF PINS

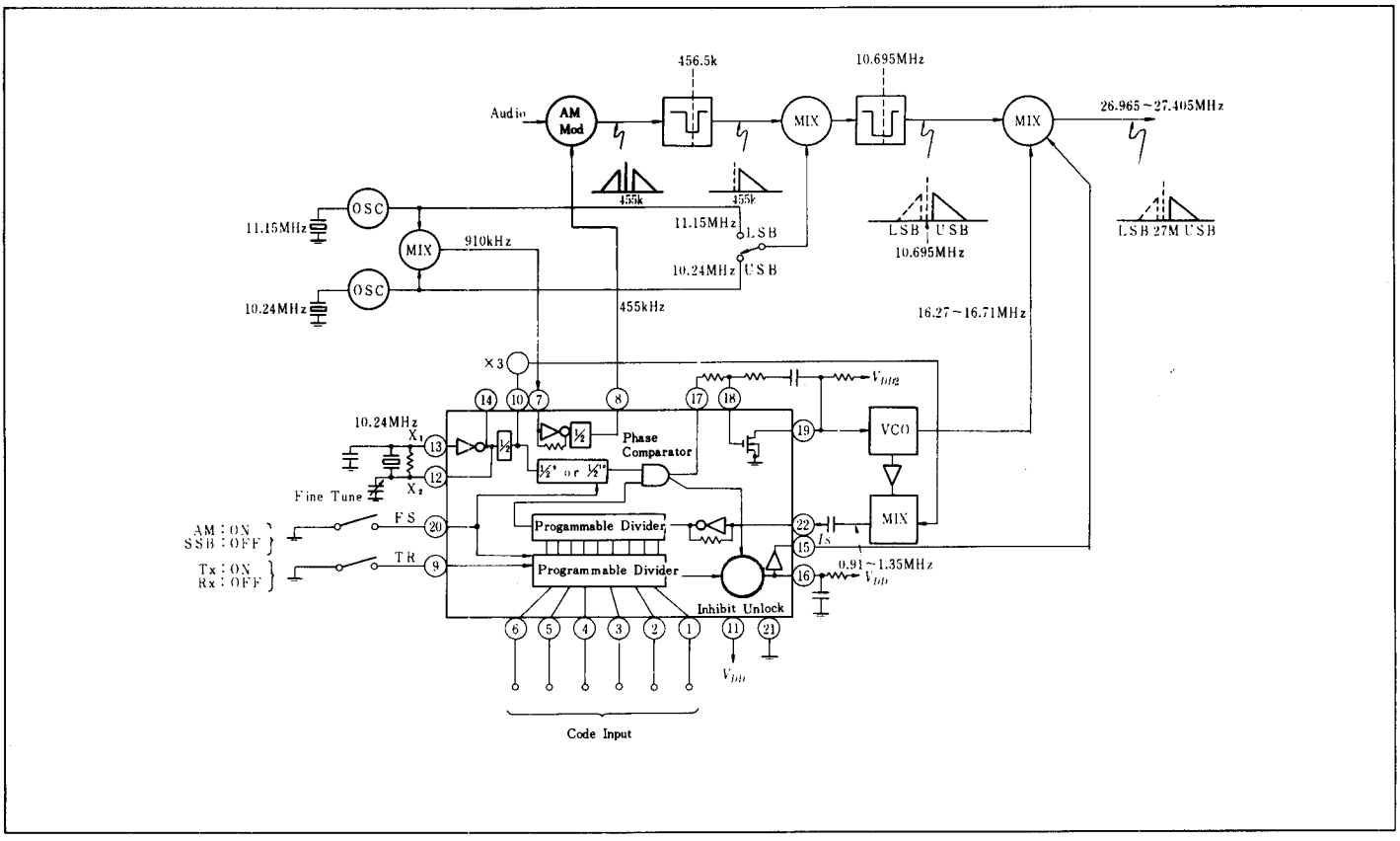
Pin No.	Markings	Names	Functions
①	P_1	BCD programming input	Input pin for 2^0 of single figure Pull-down resister, incorporated
②	P_2	BCD programming input	Input pin for 2^1 of single figure Pull-down resister incorporated
③	P_3	BCD programming input	Input pin for 2^2 of single figure Pull-down resister incorporated
④	P_4	BCD programming input	Input pin for 2^3 of single figure Pull-down resister incorporporated
⑤	P_5	BCD programming input	Input pin for 2^0 of double figures Pull-down resister incorporated
⑥	P_6	BCD programming input	Input pin for 2^1 of double figures Pull-down resister incorporated
⑦	T	Toggle input	Input pin for 1/2 divider for use with SSB/Internally biased/Operable to sine wave 0.28V_{P-P} min, f = 6MHz
⑧	Q	1/2 divider output	Output pin for 1/2 divider for use with SSB
⑨	TR	Switching between transmission and reception	Pin for switching between transmission and reception. To become code for reception when released and for transmission when grounded. To be counted same when FS pin is released
⑩	D_2	5.12MHz output	1/2 divider output of 10.24MHz
⑪	V_{DD}	Power supply	Maximum ratings 6.0V. Operation voltage 4.5 to 5.5V
⑫	X_2	Crystal input	10.24MHz X-tal terminal. On output side of OSC inverter. Feedback resistor with X_1, being external
⑬	X_1	Crystal input	10.24MHz X-tal terminal. On input side of OSC inverter
⑭	X_B	Crystal output buffer	10.24MHz oscillation signal output Buffer incorporated
⑮	IS	Instant stop output	To go to low level during unlocking and off-channel programming
⑯	TC	Timing input for IS	IS pin filter terminal. Drain of n-channel MOS
⑰	EO	ϕ-Detection output	Phase detection output pin. Charge pump incorporated
⑱	AI	Active filter amplifier input	Gate of active filter n-channel MOS
⑲	AO	Active filter amplifier output	Drain of active filter n-channel MOS. Voltage resistance 20V
⑳	FS	5k/10kHz switching	Switching 10.24MHz oscillation signal to 1024 (10kHz and 1/2048 [5kHz]). 10kHz when released and 5kHz when grounded
㉑	GND	Ground	
㉒	PI	Programmable divider input	Internally biased. Maximum input frequency 3.3MHz. Input signal 0.28V_{P-P} min

■ CODING CHART

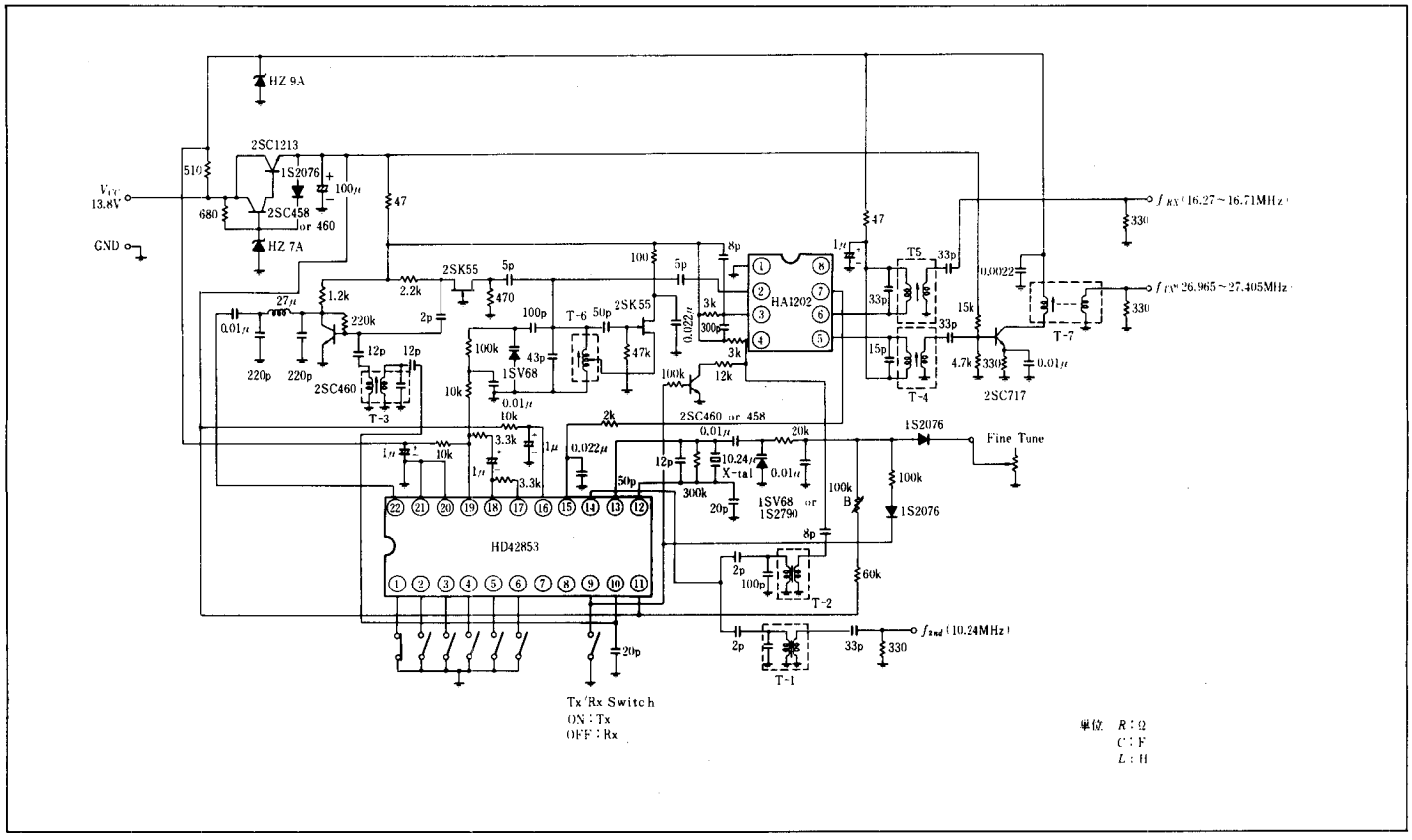
Channel	Code Input						IS Output	at AM Reception TR=1, FS=0 (Dvider Output 5kHz)		at AM Transmission TR=0, FS=0 (Divider Output 5kHz)		at SSB Reception TR=X, FS=1 (Divider Output 10kHz)	
	⑥	⑤	④	③	②	①	⑮	programmable Divider N	VCO Frequency	Programmable Divider N	VCO Frequency	Programmable Divider N	VCO Frequency
1	0	0	0	0	0	1	1	182	16.27 (MHz)	273	16.725 (MHz)	91	16.27 (MHz)
2	0	0	0	0	1	0	1	184	28	275	735	92	28
3	0	0	0	0	1	1	1	186	29	277	745	93	29
4	0	0	0	1	0	0	1	190	31	281	765	95	31
5	0	0	0	1	0	1	1	192	32	283	775	96	32
6	0	0	0	1	1	0	1	194	33	285	785	97	33
7	0	0	0	1	1	1	1	196	34	287	795	98	34
8	0	0	1	0	0	0	1	200	36	291	815	100	36
9	0	0	1	0	0	1	1	202	37	293	825	101	37
10	0	1	0	0	0	0	1	204	38	295	835	102	38
11	0	1	0	0	0	1	1	206	39	297	845	103	39
12	0	1	0	0	1	0	1	210	41	301	865	105	41
13	0	1	0	0	1	1	1	212	42	303	875	106	42
14	0	1	0	1	0	0	1	214	43	305	885	107	43
15	0	1	0	1	0	1	1	216	44	307	895	108	44
16	0	1	0	1	1	0	1	220	46	311	915	110	46
17	0	1	0	1	1	1	1	222	47	313	925	111	47
18	0	1	1	0	0	0	1	224	48	315	935	112	48
19	0	1	1	0	0	1	1	226	49	317	945	113	49
20	1	0	0	0	0	0	1	230	51	321	965	115	51
21	1	0	0	0	0	1	1	232	52	323	975	116	52
22	1	0	0	0	1	0	1	234	53	325	985	117	53
23	1	0	0	0	1	1	1	240	56	331	17.015	120	56
24	1	0	0	1	0	0	1	236	54	327	16.995	118	54
25	1	0	0	1	0	1	1	238	55	329	17.005	119	55
26	1	0	0	1	1	0	1	242	57	333	025	121	57
27	1	0	0	1	1	1	1	244	58	335	035	122	58
28	1	0	1	0	0	0	1	246	59	337	045	123	59
29	1	0	1	0	0	1	1	248	60	339	055	124	60
30	1	1	0	0	0	0	1	250	61	341	065	125	61
31	1	1	0	0	0	1	1	252	62	343	075	126	62
32	1	1	0	0	1	0	1	254	63	345	085	127	63
33	1	1	0	0	1	1	1	256	64	347	095	128	64
34	1	1	0	1	0	0	1	258	65	349	105	129	65
35	1	1	0	1	0	1	1	260	66	351	115	130	66
36	1	1	0	1	1	0	1	262	67	353	125	131	67
37	1	1	0	1	1	1	1	264	68	355	135	132	68
38	1	1	1	0	0	0	1	266	69	357	145	133	69
39	1	1	1	0	0	1	1	268	70	359	155	134	70
40	0	0	0	0	0	0	1	270	71	361	165	135	71
	×	×	1	×	1	×	0	182	27	273	16.725	91	27
	×	×	1	1	0	×	0	182	27	273	725	91	27

Note: × indicates 0 and 1. (0:GND, 1:V_{DD})

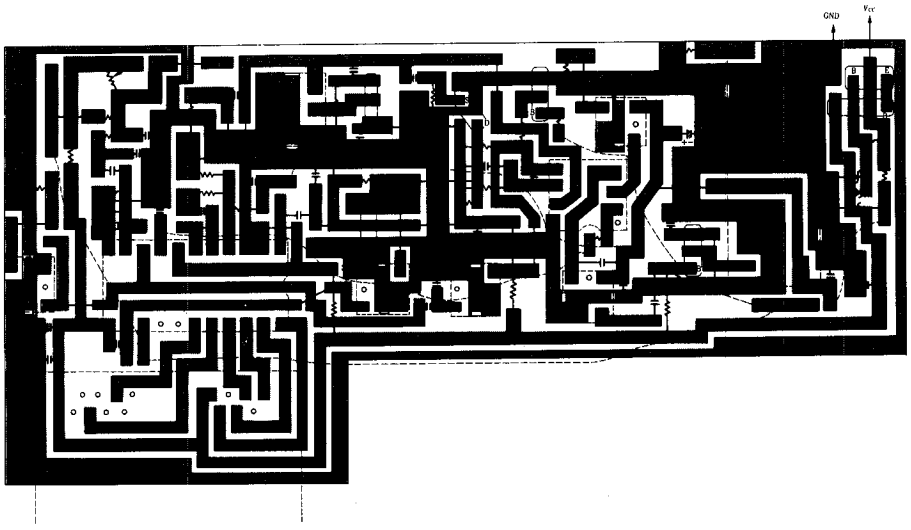
■ SSB SYSTEM



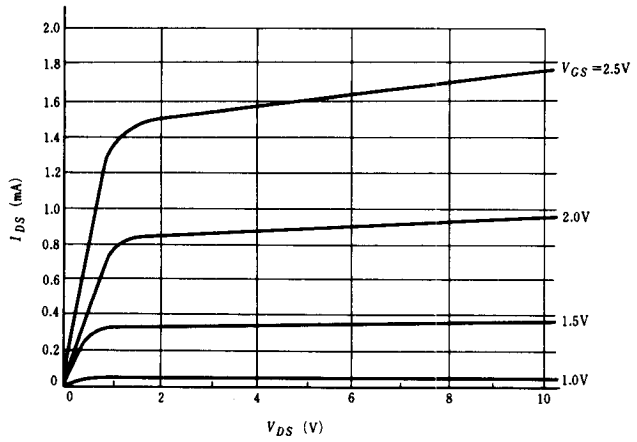
■ CIRCUIT EXAMPLE-AM SYSTEM



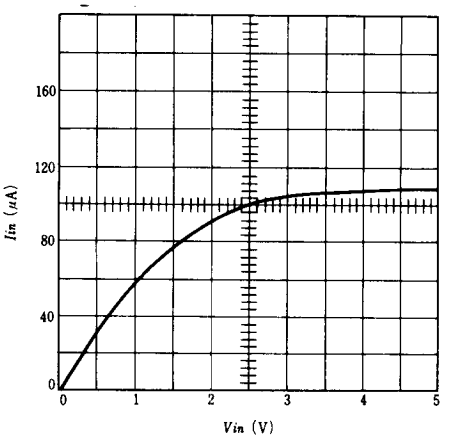
■ PC-BOARD LAYOUT PATTERN



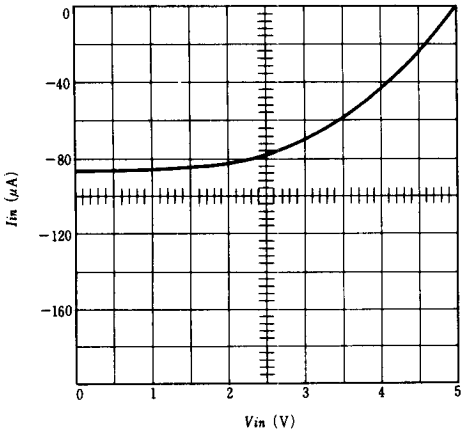
STATIC CHARACTERISTICS OF ACTIVE FILTER AMPLIFIER



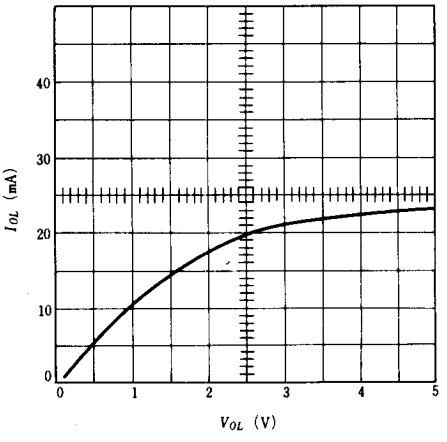
PULL-DOWN RESISTANCE 1 to 6 PINS V_{DD}=5.0V



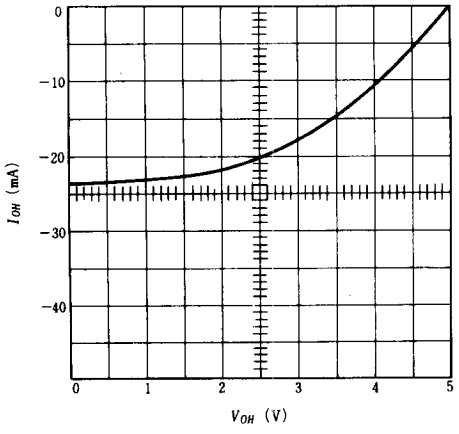
PULL-UP RESISTANCE 9, 20 PINS V_{DD}=5.0V



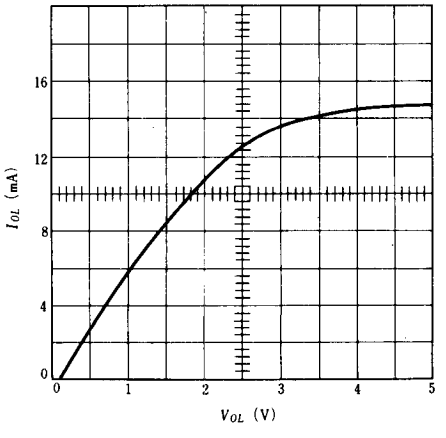
⑭ PIN I_{OL}-V_{OL}



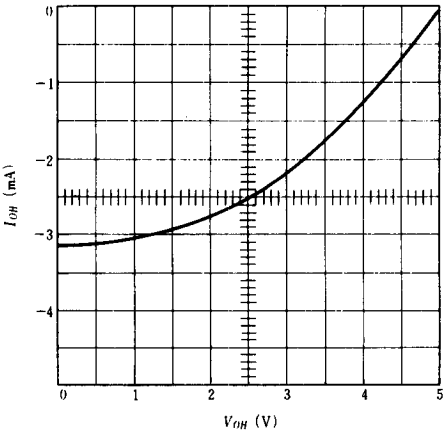
14 PIN I_{OH}-V_{OH}



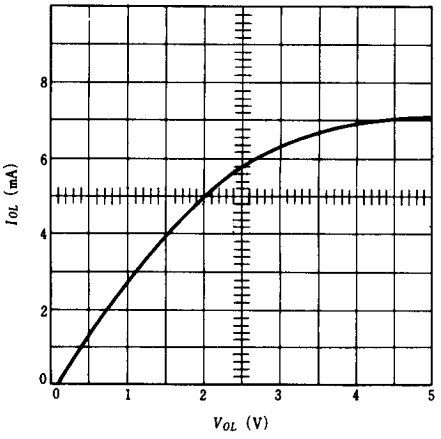
⑩ PIN I_{OL}-V_{OL}



(10) PIN I_{OH}-V_{OH}



(8) PIN I_{OL}-V_{OL}



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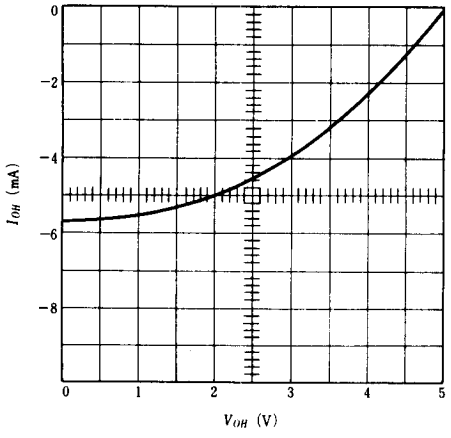
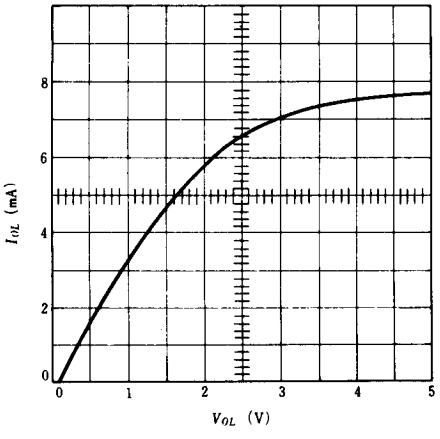
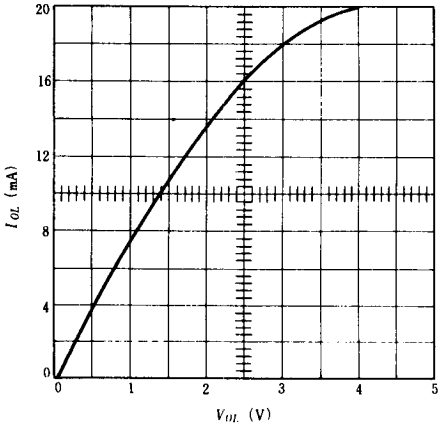


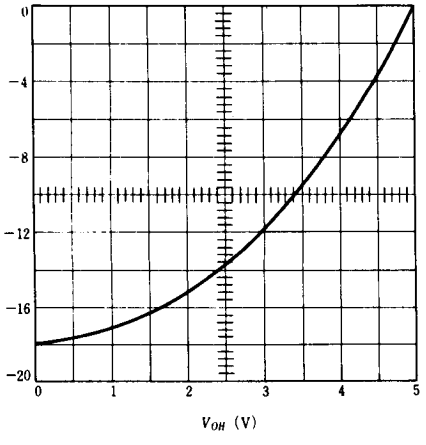
(16) PIN I_{OL}-V_{OL}



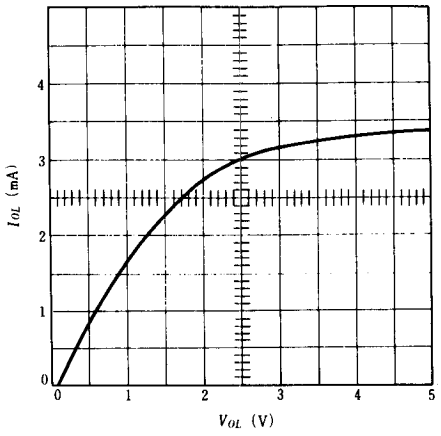
(15) PIN I_{OL}-V_{OL}



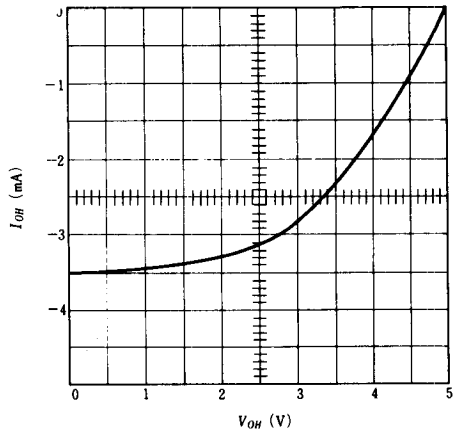
(15) PIN I_{OH}-V_{OH}



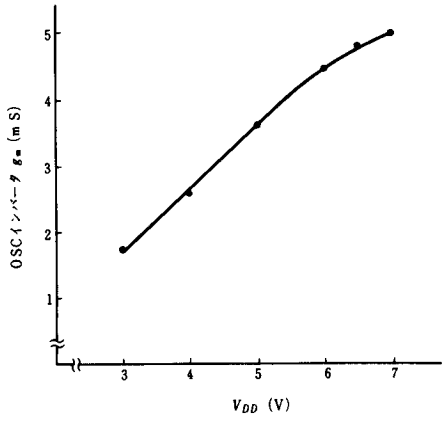
⑰ PIN I_{OL}-V_{OL}



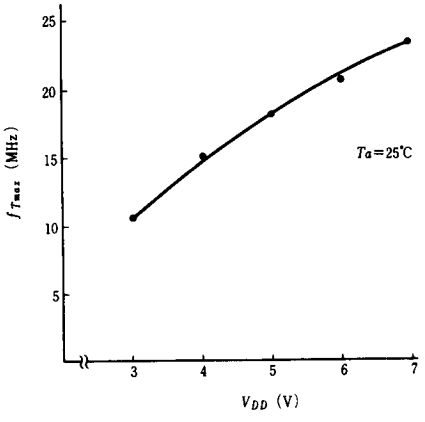
⑰ PIN I_{OH}-V_{OH}



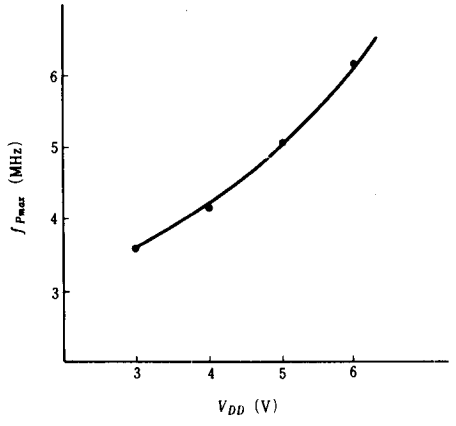
OSC INVERTER gm CHARACTERISTICS



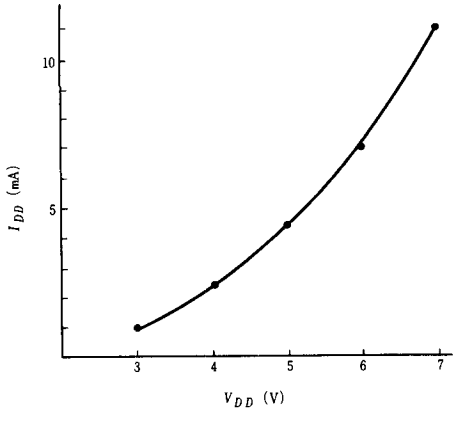
$f_T$max CHARACTERISTICS



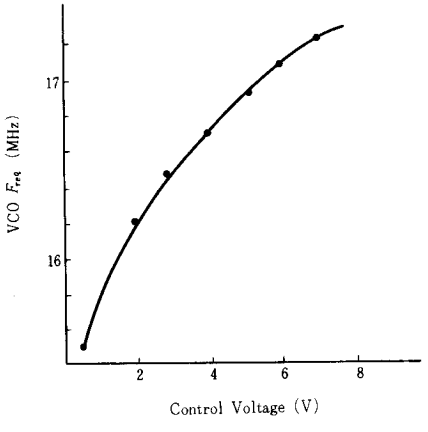
$f_P$max-V_{DD} CHARACTERISTICS



I_{DD}-V_{DD} CHARACTERISTICS



VCO CHARACTERISTICS



SPURIOUS CHARACTERISTICS OF PLL BASE PLATE